FEATURES

- **ST16C654/654D Pin Compatible With Additional Enhancements**
- **Support Up To 24-MHz Crystal Input Clock (1.5 Mbps)**
- **Support Up To 48-MHz Oscillator Input Clock (3 Mbps) for 5-V Operation**
- **Support Up To 32-MHz Oscillator Input Clock (2 Mbps) for 3.3-V Operation**
- **Support Up To 24-MHz Input Clock (1.5 Mbps) for 2.5-V Operation**
- **Support Up To 16-MHz Input Clock (1 Mbps) for 1.8-V Operation**
- **64-Byte Transmit FIFO**
- **64-Byte Receive FIFO With Error Flags**
- **Programmable and Selectable Transmit and Receive FIFO Trigger Levels for DMA and Interrupt Generation**
- **Programmable Receive FIFO Trigger Levels for Software/Hardware Flow Control**
- **Software/Hardware Flow Control**
  - **Programmable Xon/Xoff Characters**
  - **Programmable Auto-$\overline{\text{RTS}}$ and Auto-$\overline{\text{CTS}}$**
- **Optional Data Flow Resume by Xon Any Character**
- **DMA Signaling Capability for Both Received and Transmitted Data on PN Package**
- **RS-485 Mode Support**
- **Support 1.8-V, 2.5-V, 3.3-V or 5-V Supply**
- **Characterized for Operation From –40°C to 85°C, Available in Commercial and Industrial Temperature Grades**
- **Software Selectable Baud Rate Generator**
- **Prescalable Provides Additional Divide by 4 Function**
- **Programmable Sleep Mode**
- **Programmable Serial Interface Characteristics**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even, Odd, or No Parity Bit Generation and Detection**
  - **1-, 1.5-, or 2-Stop Bit Generation**
- **False Start Bit Detection**
- **Complete Status Reporting Capabilities in Both Normal and Sleep Mode**
- **Line Break Generation and Detection**
- **Internal Test and Loopback Capabilities**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions ($\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$, and $\overline{\text{CD}}$)**
- **IrDA Capability**

DESCRIPTION

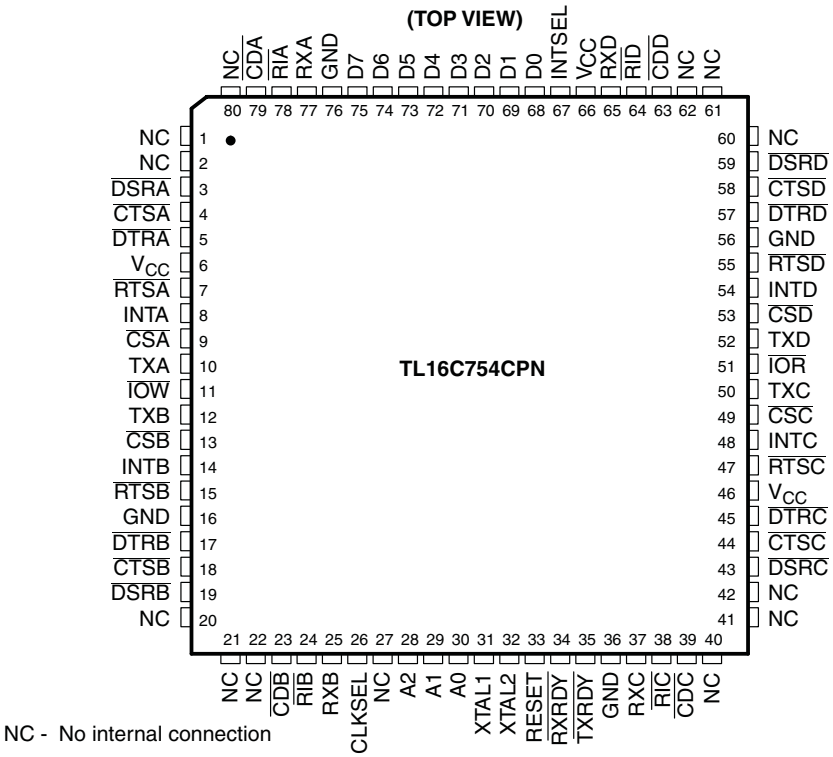
The '754C is a quad universal asynchronous receiver/transmitter (UART) with 64-byte FIFOs, automatic hardware/software flow control, and data rates up to 3 Mbps. It incorporates the functionality of four UARTs, each UART having its own register set and FIFOs. The four UARTs share only the data bus interface and clock source, otherwise they operate independently. Another name for the UART function is Asynchronous Communications Element (ACE), and these terms are used interchangeably. The bulk of this document describes the behavior of each ACE, with the understanding that four such devices are incorporated into the '754C. The '754C offers enhanced features. It has a transmission control register (TCR) that stores received FIFO threshold level to start/stop transmission during hardware and software flow control. With the FIFO RDY register, the software gets the status of TXRDY/RXRDY for all four ports in one access. On-chip status registers provide the user with error indications, operational status, and modem interface control. System interrupts may be tailored to meet user requirements. An internal loopback capability allows onboard diagnostics.

Each UART transmits data sent to it from the peripheral 8-bit bus on the TX signal and receives characters on the RX signal. Characters can be programmed to be 5, 6, 7, or 8 bits. The UART has a 64-byte receive FIFO and transmit FIFO and can be programmed to interrupt at different trigger levels. The UART generates its own desired baud rate based upon a programmable divisor and its input clock. It can transmit even, odd, or no parity and 1-, 1.5-, or 2-stop bits. The receiver can detect break, idle or framing errors, FIFO overflow, and parity errors. The transmitter can detect FIFO underflow. The UART also contains a software interface for modem control operations, and software flow control and hardware flow control capabilities.

The '754C will be available in 80-pin TQFP PN and 64-pin TQFP PM packages. The TL16CP754CPM is currently available; the TL16CM754CPM and TL16C754CPN will be available in 2008.

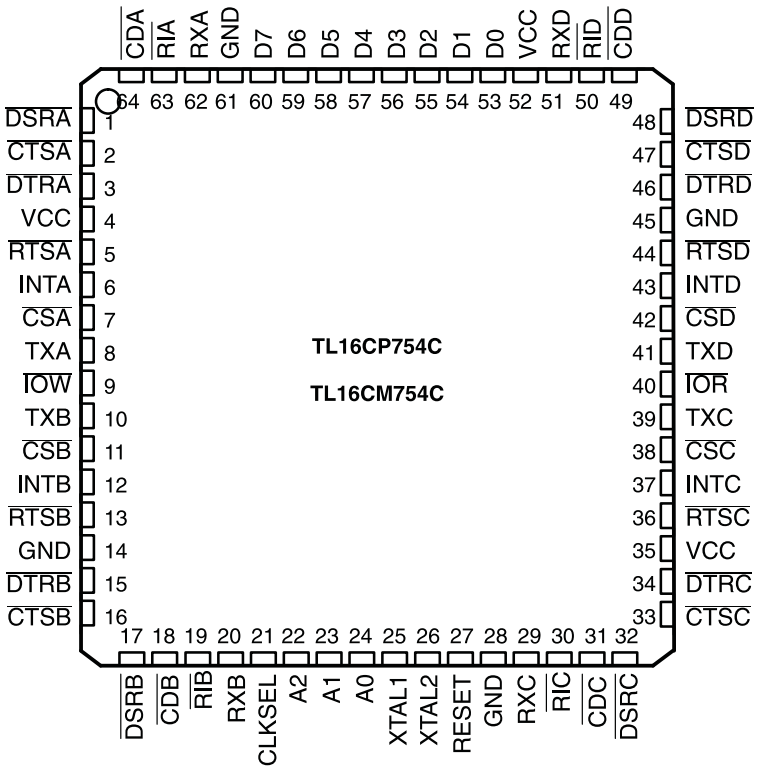
There are two versions available in the PM package, the TL16CP754C and the TL16CM754C. The 'CP754C internally connects the INTSEL signal to V_{CC} and the 'CM754C internally connects the INTSEL signal to GND.

PN PACKAGE
(TOP VIEW)



NC - No internal connection

PM PACKAGE
(TOP VIEW)



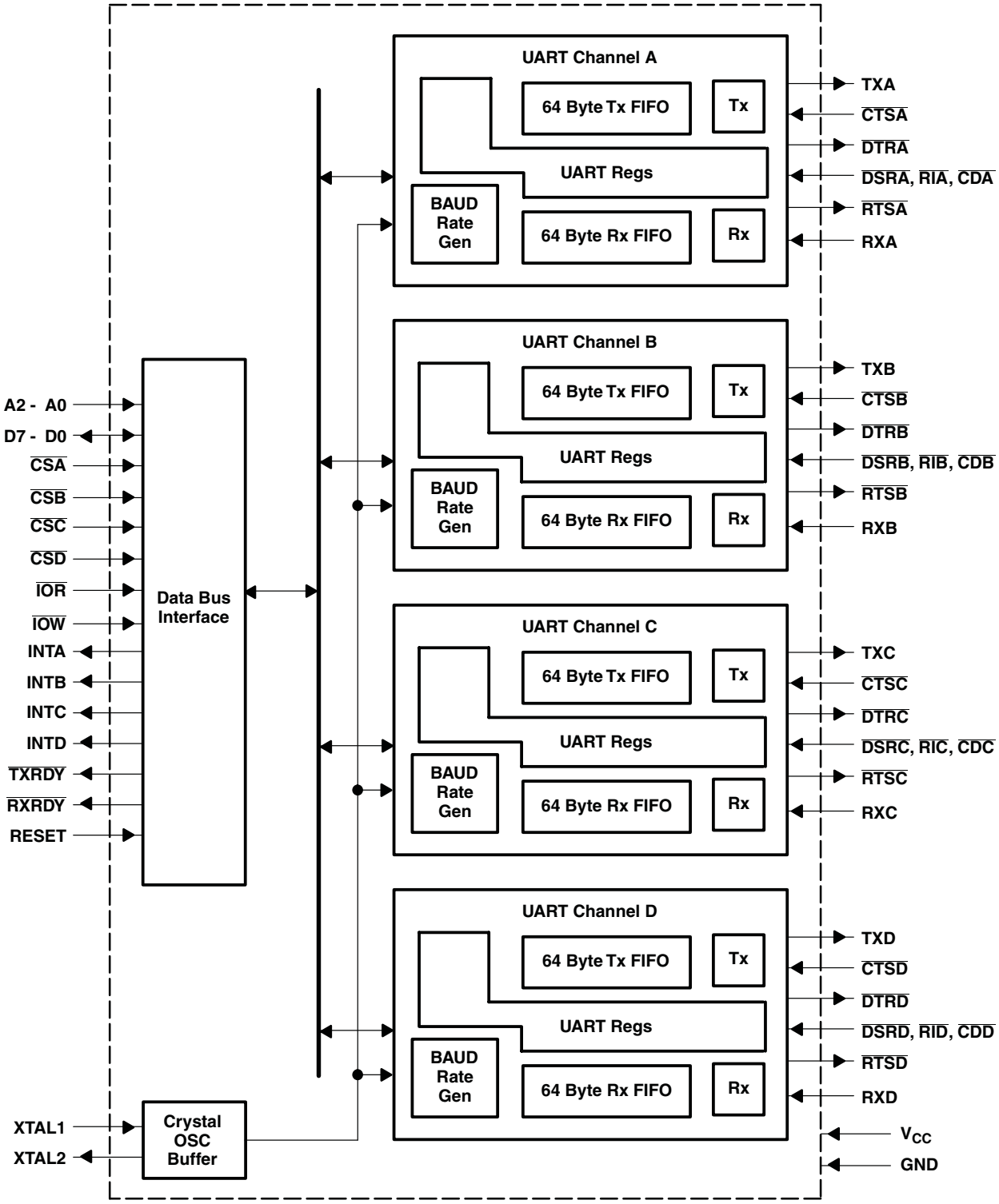
TERMINAL FUNCTIONS

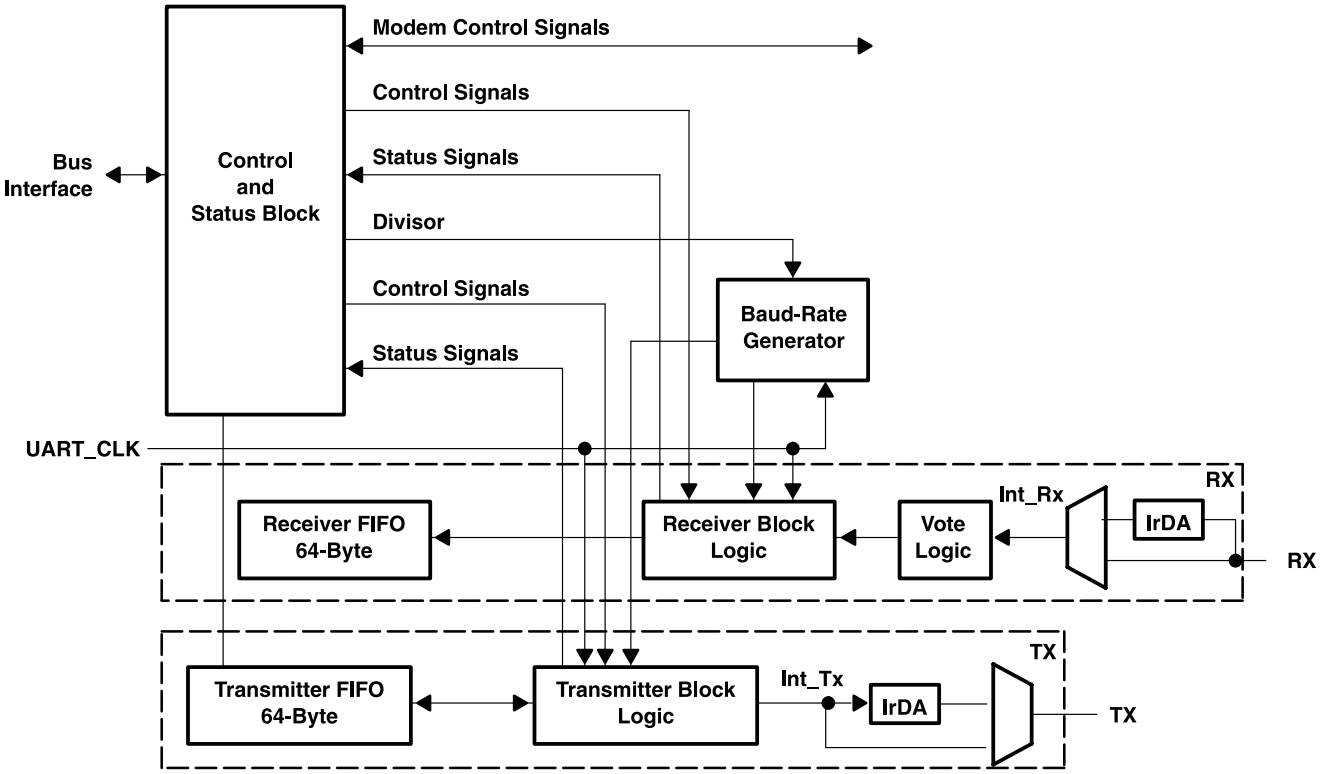
TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PN	PM		
A0	30	24	I	Address bit 0 select. Internal registers address selection. Refer to Table 7 for Register Address Map.
A1	29	23	I	Address bit 1 select. Internal registers address selection. Refer to Table 7 for Register Address Map.
A2	28	22	I	Address bit 2 select. Internal registers address selection. Refer to Table 7 for Register Address Map.
$\overline{CDA}$, $\overline{CDB}$, $\overline{CDC}$, $\overline{CDD}$	79, 23, 39, 63	64, 19, 31, 49	I	Carrier detect (active low). These inputs are associated with individual UART channels A through D. A low on these pins indicates that a carrier has been detected by the modem for that channel.
CLKSEL	26	21	I	Clock select. CLKSEL selects the divide-by-1 or divide-by-4 prescalable clock. During the reset, a logic 1 (V_{CC}) on CLKSEL selects the divide-by-1 prescaler. A logic 0 (GND) on CLKSEL selects the divide-by-4 prescaler. The value of CLKSEL is latched into MCR[7] at the trailing edge of RESET. A logic 1 (V_{CC}) on CLKSEL will latch a 0 into MCR[7]. A logic 0 (GND) on CLKSEL will latch a 1 into MCR[7]. MCR[7] can be changed after RESET to alter the prescaler value.
$\overline{CSA}$, $\overline{CSB}$, $\overline{CSC}$, $\overline{CSD}$	9, 13, 49, 53	7, 11, 38, 42	I	Chip select A, B, C, and D (active low). These pins enable data transfers between the user CPU and the '754C for the channel(s) addressed. Individual UART sections (A, B, C, D) are addressed by providing a low on the respective CSA through CSD pin.
$\overline{CTSA}$, $\overline{CTSB}$, $\overline{CTSC}$, $\overline{CTSD}$	4, 18, 44, 58	2, 16, 33, 47	I	Clear to send (active low). These inputs are associated with individual UART channels A through D. A low on the $\overline{CTS}$ pins indicates the modem or data set is ready to accept transmit data from the 754A. Status can be checked by reading MSR[4]. These pins only affect the transmit and receive operations when auto $\overline{CTS}$ function is enabled through the enhanced feature register (EFR[7]), for hardware flow control operation.
D0–D2, D3–D7	68–70, 71–75	53–60	I/O	Data bus (bidirectional). These pins are the eight-bit, 3-state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.
$\overline{DSRA}$, $\overline{DSRB}$, $\overline{DSRC}$, $\overline{DSRD}$	3, 19, 43, 59	1, 17, 32, 48	I	Data set ready (active low). These inputs are associated with individual UART channels A through D. A low on these pins indicates the modem or data set is powered on and is ready for data exchange with the UART.
$\overline{DTRA}$, $\overline{DTRB}$, $\overline{DTRC}$, $\overline{DTRD}$	5, 17, 45, 57	3, 15, 34, 46	O	Data terminal ready (active low). These outputs are associated with individual UART channels A through D. A low on these pins indicates that the 754A is powered on and ready. These pins can be controlled through the modem control register. Writing a 1 to MCR[0] sets the $\overline{DTR}$ output to low, enabling the modem. The output of these pins is high after writing a 0 to MCR[0], or after a reset. These pins can also be used in the RS-485 mode to control an external RS-485 driver or transceiver.
GND	16, 36, 56, 76	14, 28, 45, 61	Pwr	Power signal and power ground
$\overline{INTA}$, $\overline{INTB}$, $\overline{INTC}$, $\overline{INTD}$	8, 14, 48, 54	6, 12, 37, 43	O	Interrupt A, B, C, and D (active high). These pins provide individual channel interrupts, INTA-D. INTA−D are enabled when MCR[3] is set to a 1, interrupts are enabled in the interrupt enable register (IER) and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected. INTA−D are in the high-impedance state after reset.
INTSEL	67	–	I	Interrupt select (active high with internal pulldown). INTSEL can be used in conjunction with MCR[3] to enable or disable the 3-state interrupts INTA-D or override MCR[3] and force continuous interrupts. Interrupt outputs are enabled continuously by making this pin a 1. Driving this pin low allows MCR[3] to control the 3-state interrupt output. In this mode, MCR[3] is set to a 1 to enable the 3-state outputs.
$\overline{IOr}$	51	40	I	Read input (active low strobe). A valid low level on $\overline{IOR}$ loads the contents of an internal register defined by address bits A0–A2 onto the '754C data bus (D0–D7) for access by an external CPU.
$\overline{IOW}$	11	9	I	Write input (active low strobe). A valid low level on $\overline{IOW}$ transfers the contents of the data bus (D0–D7) from the external CPU to an internal register that is defined by address bits A0–A2.
RESET	33	27	I	Reset. RESET resets the internal registers and all the outputs. The UART transmitter output and the receiver input are disabled during reset time. See '754C external reset conditions for initialization details. RESET is an active high input.

TERMINAL FUNCTIONS (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PN	PM		
$\overline{RIA}$, $\overline{RIB}$, $\overline{RIC}$, $\overline{RID}$	78, 24, 38, 64	63, 19, 30, 50	I	Ring indicator (active low). These inputs are associated with individual UART channels A through D. A low on these pins indicates the modem has received a ringing signal from the telephone line. A low-to-high transition on these input pins generates a modem status interrupt, if it is enabled.
$\overline{RTSA}$, $\overline{RTSB}$, $\overline{RTSC}$, $\overline{RTSD}$	7, 15, 47, 55	5, 13, 36, 44	O	Request to send (active low). These outputs are associated with individual UART channels A through D. A low on the $\overline{RTS}$ pins indicates the transmitter has data ready and waiting to send. Writing a 1 in the modem control register (MCR[1]) sets these pins to low, indicating data is available. After a reset, these pins are set to 1. These pins only affect the transmit and receive operation when auto-$\overline{RTS}$ function is enabled through the enhanced feature register (EFR[6]), for hardware flow control operation.
$\overline{RXA}$, $\overline{RXB}$, $\overline{RXC}$, $\overline{RXD}$	77, 25, 37, 65	62, 20, 29, 51	I	Receive data input. These inputs are associated with individual serial channel data to the 754A. During the local loopback mode, these RX input pins are disabled and TX data is internally connected to the UART RX input internally. During normal mode, RXn should be held high when no data is being received. These outputs also can be used in IrDA mode. See the IrDA mode section for more information.
$\overline{RXRDY}$	34	–	O	Receive ready (active low). RXRDY contains the wire-ORed status of all four receive channel FIFOs, RXRDY A–D. It goes low when the trigger level has been reached or a timeout interrupt occurs. It goes high when all RX FIFOs are empty and there is an error in RX FIFO.
$\overline{TXA}$, $\overline{TXB}$, $\overline{TXC}$, $\overline{TXD}$	10, 12, 50, 52	8, 10, 39, 41	O	Transmit data. These outputs are associated with individual serial transmit channel data from the 754A. During the local loopback mode, the TX input pin is disabled and TX data is internally connected to the UART RX input. During normal mode, TXn is high when no data is being sent. These outputs can also be used in IrDA mode, in which case TXn is low when no data is being sent. See the IrDA mode section for more information.
$\overline{TXRDY}$	35	–	O	Transmit ready (active low). $\overline{TXRDY}$ contains the wire-ORed status of all four transmit channel FIFOs, TXRDY A–D. It goes low when there are a trigger level number of spares available. It goes high when all four TX buffers are full.
V_{CC}	6, 46, 66	4, 35, 52	Pwr	Power supply inputs
XTAL1	31	25	I	Crystal or external clock input. XTAL1 functions as a crystal input or as an external clock input. A crystal can be connected between XTAL1 and XTAL2 to form an internal oscillator circuit (see Figure 10). Alternatively, an external clock can be connected to XTAL1 to provide custom data rates.
XTAL2	32	26	O	Output of the crystal oscillator or buffered clock. See also XTAL1. XTAL2 is used as a crystal oscillator output or buffered clock output.

FUNCTIONAL BLOCK DIAGRAM





A. The vote logic determines whether the RX data is a logic 1 or 0. It takes three samples of the RX line and uses a majority vote to determine the logic level received. The Vote logic operates on all bits received.

FUNCTIONAL DESCRIPTION

The '754C UART is pin compatible with the TL16C554 and ST16C654 UARTs. It provides more enhanced features. All additional features are provided through a special enhanced feature register.

The UART performs serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-parallel conversion on data characters transmitted by the processor. The complete status of each channel of the '754C UART can be read at any time during functional operation by the processor.

The '754C UART can be placed in an alternate mode (FIFO mode) relieving the processor of excessive software overhead by buffering received/transmitted characters. Both the receiver and transmitter FIFOs can store up to 64 bytes (including three additional bits of error status per byte for the receiver FIFO) and have selectable or programmable trigger levels. Primary outputs RXRDY and TXRDY allow Signaling of DMA transfers.

The '754C UART has selectable hardware flow control and software flow control. Both schemes significantly reduce software overhead and increase system efficiency by automatically controlling serial data flow. Hardware flow control uses the $\overline{RTS}$ output and $\overline{CTS}$ input signals. Software flow control uses programmable Xon/Xoff characters.

The UART includes a programmable baud rate generator that can divide the timing reference clock input by a divisor between 1 and (2^{16}–1). The CLKSEL pin can be used to divide the input clock by 4 or by 1 to generate the reference clock during the reset. The divide-by-4 clock is selected when CLKSEL pin is a logic 0 or the divide-by-1 is selected when CLKSEL is a logic 1.

Trigger Levels

The '754C UART provides independent selectable and programmable trigger levels for both receiver and transmitter DMA and interrupt generation. After reset, both transmitter and receiver FIFOs are disabled and so, in effect, the trigger level is the default value of one byte. The selectable trigger levels are available via the FCR. The programmable trigger levels are available via the TLR.

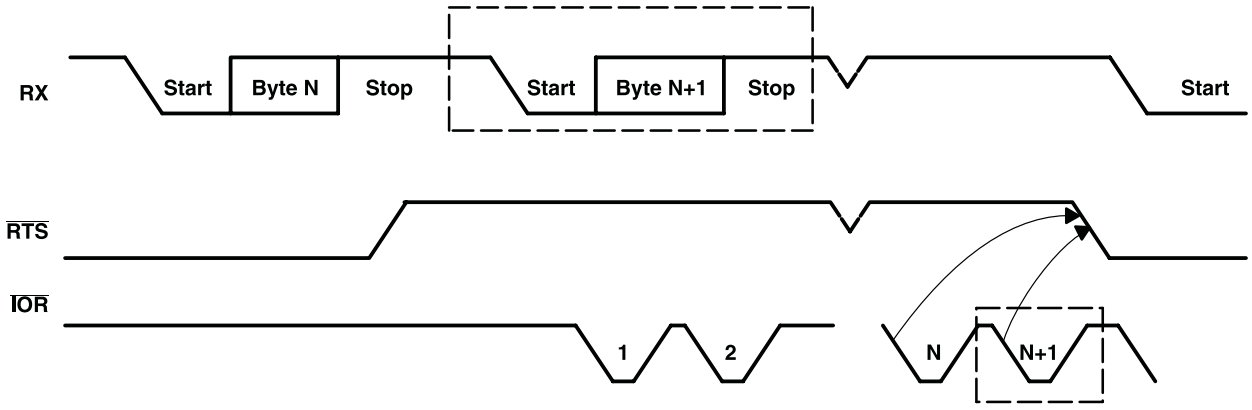
Hardware Flow Control

Hardware flow control is composed of auto-$\overline{CTS}$ and auto-$\overline{RTS}$. Auto-$\overline{CTS}$ and auto-$\overline{RTS}$ can be enabled/disabled independently by programming EFR[7:6].

With auto-$\overline{CTS}$, $\overline{CTS}$ must be active before the UART can transmit data. Auto-$\overline{RTS}$ only activates the $\overline{RTS}$ output when there is enough room in the FIFO to receive data and deactivates the $\overline{RTS}$ output when the RX FIFO is sufficiently full. The HALT and RESTORE trigger levels in the TCR determine the levels at which $\overline{RTS}$ is activated/deactivated. If both auto-$\overline{CTS}$ and auto-$\overline{RTS}$ are enabled, when $\overline{RTS}$ is connected to $\overline{CTS}$, data transmission does not occur unless the receiver FIFO has empty space. Thus, overrun errors are eliminated during hardware flow control. If not enabled, overrun errors occur if the transmit data rate exceeds the receive FIFO servicing latency.

Auto-$\overline{RTS}$

Auto-$\overline{RTS}$ data flow control originates in the receiver block (see functional block diagram). Figure 1 shows $\overline{RTS}$ functional timing. The receiver FIFO trigger levels used in Auto-$\overline{RTS}$ are stored in the TCR. $\overline{RTS}$ is active if the RX FIFO level is below the HALT trigger level in TCR[3:0]. When the receiver FIFO HALT trigger level is reached, $\overline{RTS}$ is deasserted. The sending device (e.g., another UART) may send an additional byte after the trigger level is reached (assuming the sending UART has another byte to send) because it may not recognize the deassertion of $\overline{RTS}$ until it has begun sending the additional byte. $\overline{RTS}$ is automatically reasserted once the receiver FIFO reaches the RESUME trigger level programmed via TCR[7:4]. This reassertion allows the sending device to resume transmission.



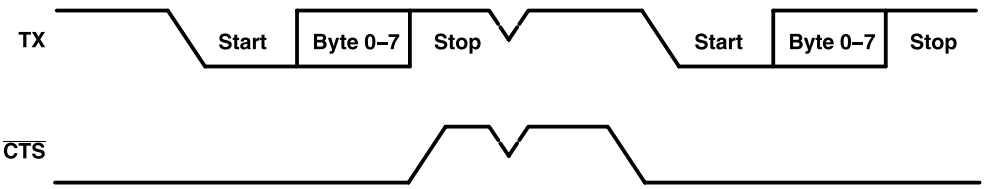
A. N = receiver FIFO trigger level B.

B. The two blocks in dashed lines cover the case where an additional byte is sent as described in Auto-$\overline{RTS}$.

Figure 1. $\overline{RTS}$ Functional Timing

Auto-$\overline{CTS}$

The transmitter circuitry checks $\overline{CTS}$ before sending the next data byte. When $\overline{CTS}$ is active, the transmitter sends the next byte. To stop the transmitter from sending the following byte, $\overline{CTS}$ must be deasserted before the middle of the last stop bit that is currently being sent. The auto-$\overline{CTS}$ function reduces interrupts to the host system. When flow control is enabled, the $\overline{CTS}$ state changes and need not trigger host interrupts because the device automatically controls its own transmitter. Without auto-$\overline{CTS}$, the transmitter sends any data present in the transmit FIFO and a receiver overrun error can result. Figure 2 shows $\overline{CTS}$ functional timing, and Figure 3 shows an example of autoflow control.



A. When $\overline{CTS}$ is low, the transmitter keeps sending serial data out.

B. When $\overline{CTS}$ goes high before the middle of the last stop bit of the current byte, the transmitter finishes sending the current byte, but it does not send the next byte.

C. When $\overline{CTS}$ goes from high to low, the transmitter begins sending data again.

Figure 2. $\overline{CTS}$ Functional Timing

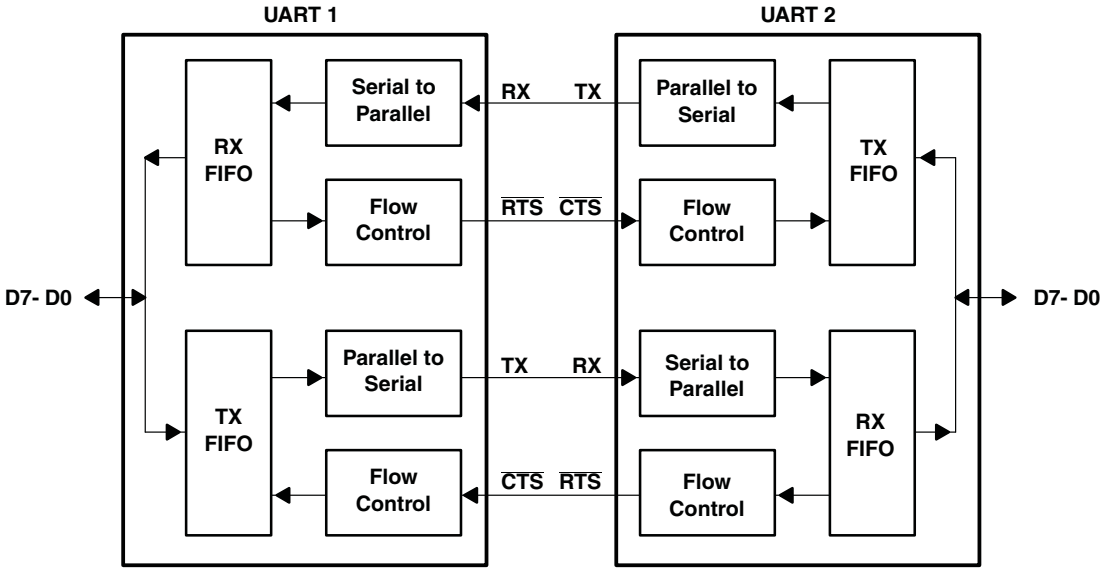


Figure 3. Autoflow Control (Auto-$\overline{RTS}$ and Auto-$\overline{CTS}$) Example

Software Flow Control

Software flow control is enabled through the enhanced feature register and the modem control register. Different combinations of software flow control can be enabled by setting different combinations of EFR[3−0]. Table 1 shows software flow control options.

Two other enhanced features relate to S/W flow control:

- **Xon Any Function [MCR(5)**: Operation resumes after receiving any character after recognizing the Xoff character.

NOTE:

It is possible that an Xon1 character is recognized as an Xon Any character, which could cause an Xon2 character to be written to the RX FIFO.

- **Special Character [EFR(5)]**: Incoming data is compared to Xoff2. Detection of the special character sets the Xoff interrupt {IIR(4)] but does not halt transmission. The Xoff interrupt is cleared by a read of the IIR. The special character is transferred to the RX FIFO.

Table 1. Software Flow Control Options EFR[3:0]

BIT 3	BIT 2	BIT 1	BIT 0	Tx, Rx SOFTWARE FLOW CONTROLS
0	0	X	X	No transmit flow control
1	0	X	X	Transmit Xon1, Xoff1
0	1	X	X	Transmit Xon2, Xoff2
1	1	X	X	Transmit Xon1, Xon2: Xoff1, Xoff2
X	X	0	0	No receive flow control
X	X	1	0	Receiver compares Xon1, Xoff1 X X 0 1
X	X	0	1	Receiver compares Xon2, Xoff2
1	0	1	1	Transmit Xon1, Xoff1 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
0	1	1	1	Transmit Xon2, Xoff2 Receiver compares Xon1 or Xon2, Xoff1 or Xoff2
1	1	1	1	Transmit Xon1, Xon2: Xoff1, Xoff2 Receiver compares Xon1 and Xon2: Xoff1 and Xoff2
0	0	1	1	No transmit flow control Receiver compares Xon1 and Xon2: Xoff1 and Xoff2

When software flow control operation is enabled, the '754C compares incoming data with Xoff1/2 programmed characters (in certain cases Xoff1 and Xoff2 must be received sequentially(1)). When an Xoff character is received, transmission is halted after completing transmission of the current character. Xoff character detection also sets IIR[4] and causes INT to go high (if enabled via IER[5]).

To resume transmission an Xon1/2 character must be received (in certain cases Xon1 and Xon2 must be received sequentially). When the correct Xon characters are received IIR[4] is cleared and the Xoff interrupt disappears.

NOTE:

If a parity, framing or break error occurs while receiving a software flow control character, this character is treated as normal data and is written to the RCV FIFO.

Xoff1/2 characters are transmitted when the RX FIFO has passed the programmed trigger level TCR[3:0].

Xon1/2 characters are transmitted when the RX FIFO reaches the trigger level programmed via TCR[7:4].

NOTE:

If, after an Xoff character has been sent, software flow control is disabled, the UART transmits Xon characters automatically to enable normal transmission to proceed. A feature of the '754C UART design is that if the software flow combination (EFR[3:0]) changes after an Xoff has been sent, the originally programmed Xon is automatically sent. If the RX FIFO is still above the trigger level the newly programmed Xoff1/2 is transmitted.

The transmission of Xoff/Xon(s) follows the exact same protocol as transmission of an ordinary byte from the FIFO. This means that even if the word length is set to be 5, 6, or 7 characters, then the 5, 6, or 7 least significant bits of Xoff1,2/Xon1,2 are transmitted. The transmission of 5, 6, or 7 bits of a character is seldom done, but this functionality is included to maintain compatibility with earlier designs.

It is assumed that software flow control and hardware flow control are never enabled simultaneously. Figure 4 shows a software flow control example.

(1) When pairs of Xon/Xoff characters are programmed to occur sequentially, received Xon1/Xoff1 characters will be written to the Rx FIFO if the subsequent character is not Xon2/Xoff2.

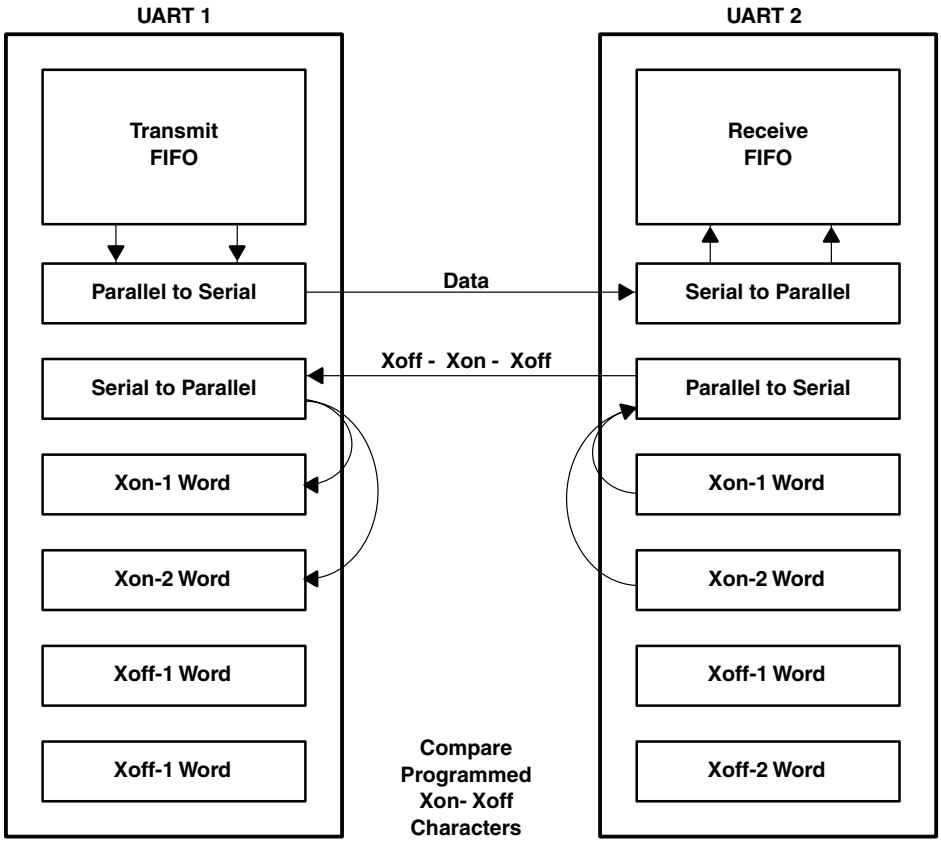


Figure 4. Software Flow Control Example

Software Flow Control Example

Assumptions: UART1 is transmitting a large text file to UART2. Both UARTs are using software flow control with single character Xoff (0F) and Xon (0D) tokens. Both have Xoff threshold (TCR [3:0]=F) set to 60 and Xon threshold (TCR[7:4]=8) set to 32. Both have the interrupt receive threshold (TLR[7:4]=D) set to 52.

UART1 begins transmission and sends 52 characters, at which point UART2 generates an interrupt to its processor to service the RCV FIFO, but assumes the interrupt latency is fairly long. UART1 continues sending characters until a total of 60 characters have been sent. At this time UART2 will transmit a 0F to UART1, informing UART1 to halt transmission. UART1 will likely send the 61st character while UART2 is sending the Xoff character. Now UART2 is serviced and the processor reads enough data out of the RCV FIFO that the level drops to 32. UART2 now sends a 0D to UART1, informing UART1 to resume transmission.

Reset

Table 2 summarizes the state of outputs after reset.

Table 2. Register Reset Functions(1)

REGISTER	RESET CONTROL	RESET STATE
Interrupt enable register	RESET	All bits cleared
Interrupt identification register	RESET	Bit 0 is set. All other bits cleared.
FIFO control register	RESET	All bits cleared
Line control register	RESET	Reset to 00011101 (1D hex).
Modem control register	RESET	Bit 6–0 cleared. Bit 7 reflects the inverse of the CLKSEL pin value.
Line status register	RESET	Bits 5 and 6 set. All other bits cleared.
Modem status register	RESET	Bits 0–3 cleared. Bits 4–7 input signals.
Enhanced feature register	RESET	Bit 6–0 is cleared. Bit 7 reflects the inverse of the CLKSEL pin value.
Receiver holding register	RESET	Pointer logic cleared
Transmitter holding register	RESET	Pointer logic cleared
Transmission control register	RESET	All bits cleared
Trigger level register	RESET	All bits cleared
Alternate function register	RESET	All bits (except AFR4) cleared; AFR4 set

(1) Registers DLL, DLH, SPR, Xon1, Xon2, Xoff1, Xoff2 are not reset by the top-level reset signal RESET, i.e., they hold their initialization values during reset.

Table 3 summarizes the state of outputs after reset.

Table 3. Signal Reset Functions

SIGNAL	RESET CONTROL	RESET STATE
TX	RESET	High
$\overline{\text{RTS}}$	RESET	High
$\overline{\text{DTR}}$	RESET	High
$\overline{\text{RXRDY}}$	RESET	High
$\overline{\text{TXRDY}}$	RESET	Low

Interrupts

The '754C UART has interrupt generation and prioritization (six prioritized levels of interrupts) capability. The interrupt enable register (IER) enables each of the six types of interrupts and the INT signal in response to an interrupt generation. The IER also can disable the interrupt system by clearing bits 0−3, 5−7. When an interrupt is generated, the interrupt identification register(IIR) indicates that an interrupt is pending and provides the type of interrupt through IIR[5−0]. Table 4 summarizes the interrupt control functions.

Table 4. Interrupt Control Functions

IIR[5–0]	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET METHOD
000001	None	None	None	None
000110	1	Receiver line status	OE, FE, PE, or BI errors occur in characters in the RX FIFO	FE < PE < BI: All erroneous characters are read from the RX FIFO. OE: Read LSR
001100	2	RX timeout	Stale data in RX FIFO	Read RHR
000100	2	RHR interrupt	DRDY (data ready) (FIFO disable) RX FIFO above trigger level (FIFO enable)	Read RHR
000010	3	THR interrupt	TFE (THR empty) (FIFO disable) TX FIFO passes above trigger level (FIFO enable)	Read IIR OR a write to the THR
000000	4	Modem status	MSR[3:0]= 0	Read MSR
010000	5	Xoff interrupt	Receive Xoff character(s)/special character	Receive Xon character(s)/Read of IIR
100000	6	$\overline{CTS}$, $\overline{RTS}$	$\overline{RTS}$ pin or $\overline{CTS}$ pin change state from active (low) to inactive (high)	Read IIR

It is important to note that for the framing error, parity error, and break conditions, LSR[7] generates the interrupt. LSR[7] is set when there is an error anywhere in the RX FIFO and is cleared only when there are no more errors remaining in the FIFO. LSR[4–2] always represent the error status for the received character at the top of the Rx FIFO. Reading the Rx FIFO updates LSR[4–2] to the appropriate status for the new character at the top of the FIFO. If the Rx FIFO is empty, then LSR[4–2] is all zeros.

For the Xoff interrupt, if an Xoff flow character detection caused the interrupt, the interrupt is cleared by an Xon flow character detection. If a special character detection caused the interrupt, the interrupt is cleared by a read of the ISR.

Interrupt Mode Operation

In interrupt mode (if any bit of IER[3:0] is1), the processor is informed of the status of the receiver and transmitter by an interrupt signal, INT. Therefore, it is not necessary to continuously poll the line status register (LSR) to see if any interrupt needs to be serviced. Figure 5 shows interrupt mode operation.

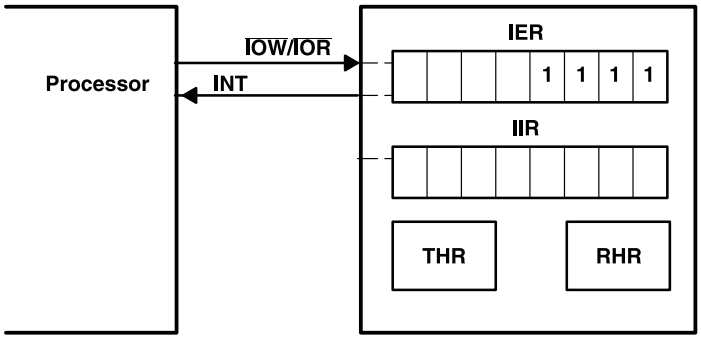


Figure 5. Interrupt Mode Operation

Polled Mode Operation

In polled mode (IER[3:0] = 0000), the status of the receiver and transmitter can then be checked by polling the line status register (LSR). This mode is an alternative to the interrupt mode of operation where the status of the receiver and transmitter is automatically known by means of interrupts sent to the CPU. Figure 6 shows polled mode operation.

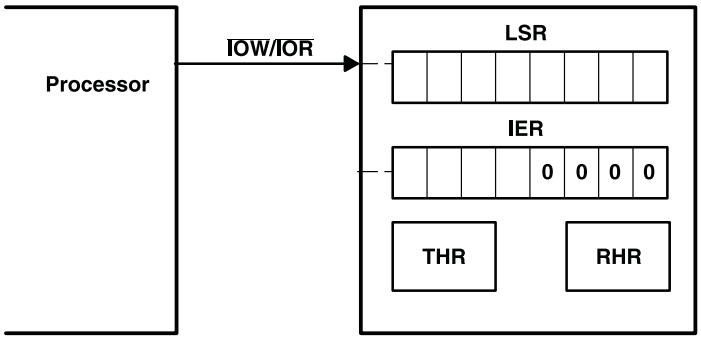


Figure 6. FIFO Polled Mode Operation

DMA Signaling

There are two modes of DMA operation, DMA mode 0 or 1, selected by FCR[3].

In DMA mode 0 or FIFO disable (FCR[0]=0) DMA occurs in single character transfers. In DMA mode 1 multicharacter (or block) DMA transfers are managed to relieve the processor for longer periods of time.

Single DMA Transfers (DMA Mode0/FIFO Disable)

Transmitter: When empty, the $\overline{\text{TXRDY}}$ signal becomes active. $\overline{\text{TXRDY}}$ goes inactive after one character has been loaded into it.

Receiver: $\overline{\text{RXRDY}}$ is active when there is at least one character in the FIFO. It becomes inactive when the receiver is empty.

Figure 7 shows $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA mode 0/FIFO disable.

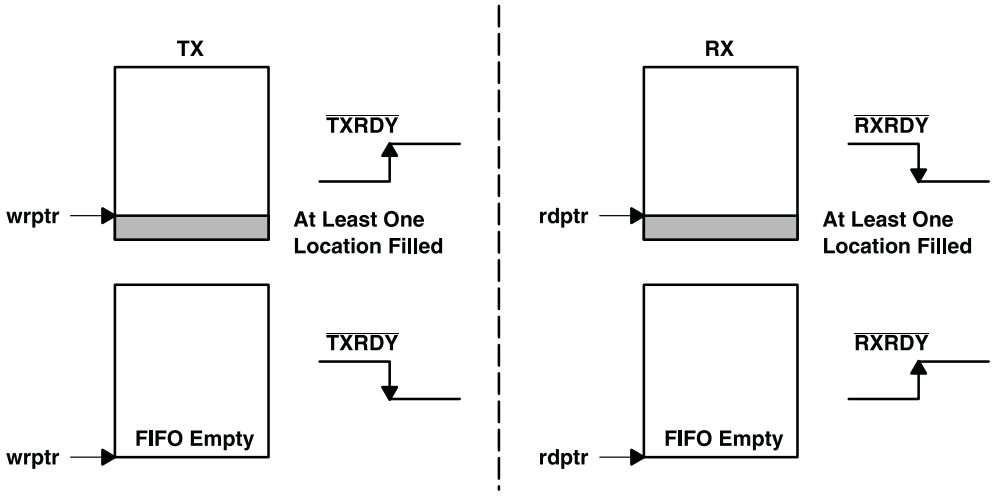


Figure 7. $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA Mode 0/FIFO Disable

Block DMA Transfers (DMA Mode1)

Transmitter: $\overline{\text{TXRDY}}$ is active when a trigger level number of spaces are available. It becomes inactive when the FIFO is full.

Receiver: $\overline{\text{RXRDY}}$ becomes active when the trigger level has been reached or when a timeout interrupt occurs. It goes inactive when the FIFO is empty or an error in the RX FIFO is flagged by LSR(7).

Figure 8 shows $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA mode 1.

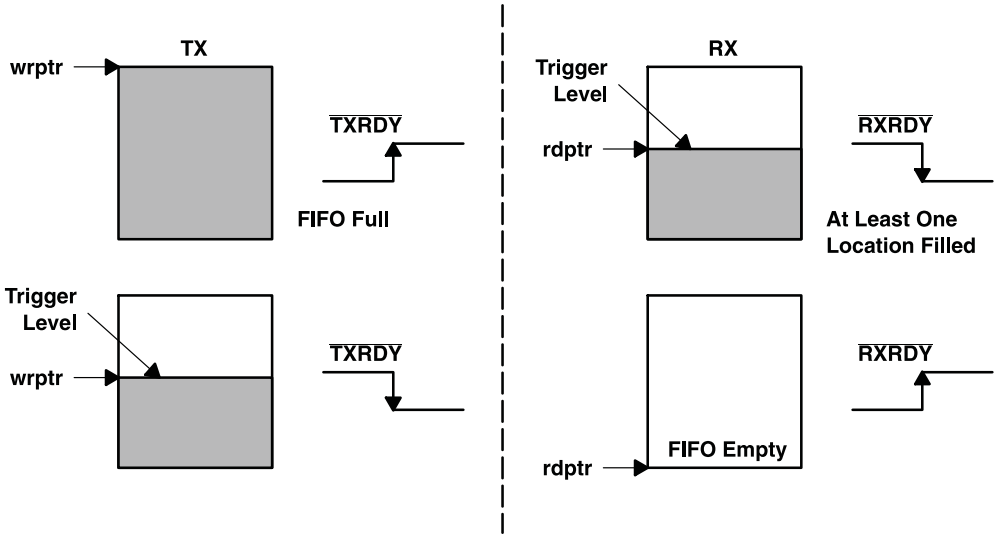


Figure 8. $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ in DMA Mode 1

Sleep Mode

Sleep mode is an enhanced feature of the '754C UART. It is enabled when EFR[4], the enhanced functions bit, is set and when IER[4] is set. Sleep mode is entered when:

- The serial data input line, RX, is idle (see break and time-out conditions).
- The TX FIFO and TX shift register are empty.
- There are no interrupts pending except THR and timeout interrupts.

Sleep mode is not entered if there is data in the RX FIFO.

In sleep mode the UART clock and baud rate clock are stopped. Because most registers are clocked using these clocks the power consumption is greatly reduced. The UART wakes up when any change is detected on the RX line, when there is any change in the state of the modem input pins or if data is written to the TX FIFO.

NOTE:

Writing to the divisor latches, DLL and DLH, to set the baud clock, must not be done during sleep mode. Therefore it is advisable to disable sleep mode using IER[4] before writing to DLL or DLH.

Break and Timeout Conditions

An RX timeout condition is detected when the receiver line, RX, has been high for a time equivalent to (4 × programmed word length) + 12 bits and there is at least one byte stored in the Rx FIFO.

When a break condition occurs, the TX line is pulled low. A break condition is activated by setting LCR[6].

Programmable Baud Rate Generator

The '754C UART contains a programmable baud generator that divides reference clock by a divisor in the range between 1 and (216−1). The output frequency of the baud rate generator is 16× the baud rate. An additional divide-by-4 prescaler is also available and can be selected by the CLKSEL pin or MCR[7], as shown in the following. The formula for the divisor is:

Divisor = (XTAL crystal input frequency / prescaler) / (desired baud rate x 16)

Where

prescaler = { 1 when CLKSEL = high during reset, or MCR[7] is set to 0 after reset
prescaler = { 4 when CLKSEL = high during reset, or MCR[7] is set to 0 after reset

Figure 9 shows the internal prescaler and baud rate generator circuitry.

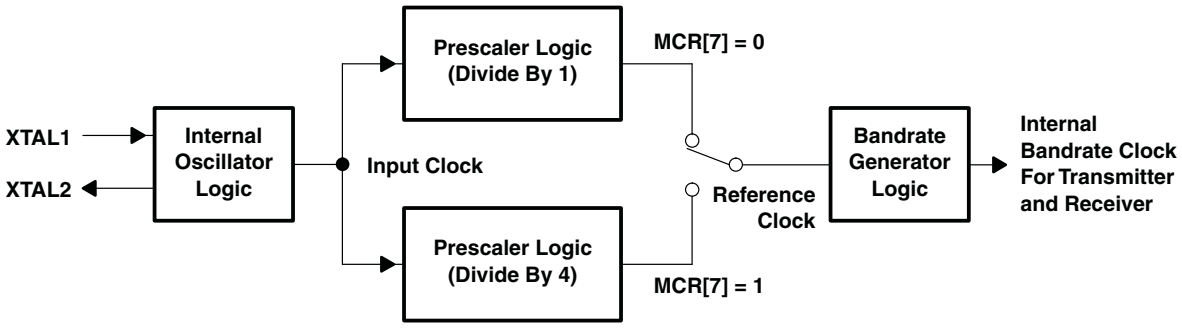


Figure 9. Prescaler and Baud Rate Generator Block Diagram

DLL and DLH must be written to in order to program the baud rate. DLL and DLH are the least significant and most significant byte of the baud rate divisor. If DLL and DLH are both zero, the UART is effectively disabled, as no baud clock is generated. The programmable baud rate generator is provided to select both the transmit and receive clock rates. Table 5 and Table 6 show the baud rate and divisor correlation for the crystal with frequency 1.8432 MHz and 3.072 MHz, respectively.

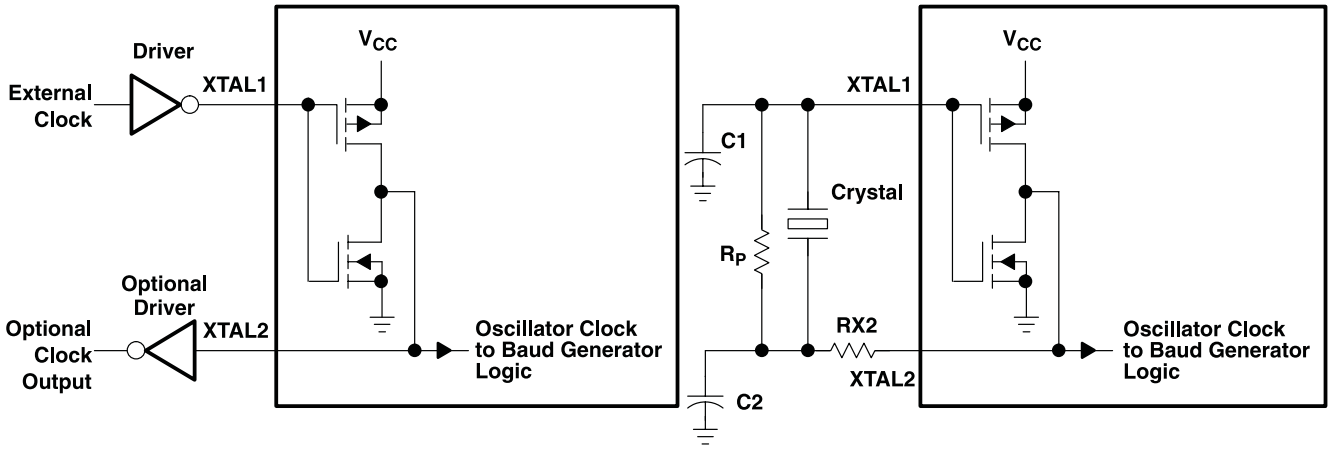
Table 5. Baud Rates Using a 1.8432-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	
75	1536	
110	1047	0.026
134.5	857	0.058
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	2.86

Table 6. Baud Rates Using a 3.072-MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16× CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	
75	2560	
110	1745	0.026
134.5	1428	0.034
150	1280	
300	640	
600	320	
1200	160	
1800	107	0.312
2000	96	
2400	80	
3600	53	0.628
4800	40	
7200	27	1.23
9600	20	
19200	10	
38400	5	

Figure 10 shows the crystal clock circuit reference.



TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	R_P	RX2	C1	C2
16 MHz	1 MΩ	0	33 pF	33 pF
3.072 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF
1.8432 MHz	1 MΩ	1.5 kΩ	10–30 pF	40–60 pF

A. For crystal with fundamental frequency from 1 MHz to 24 MHz

B. For input clock frequency higher then 24 MHz, the crystal is not allowed and the oscillator must be used, because the '754C internal oscillator cell can only support the crystal frequency up to 24 MHz.

Figure 10. Typical Crystal Clock Circuits

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range		–0.5	V_{CC} + 0.5	V
T_A	Operating free-air temperature range	TL16C754C	0	70	°C
		TL16C754CI	–40	85	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

TYPICAL PACKAGE THERMAL RESISTANCE DATA

PACKAGE		
64-pin TQFP PM	θ_{JA} = xx°C/W	θ_{JC} = xx°C/W
80-pin TQFP PN	θ_{JA} = xx°C/W	θ_{JC} = xx°C/W

TYPICAL PACKAGE WEIGHT

PACKAGE	WEIGHT IN GRAMS
64-pin TQFP PM	0.25
80-pin TQFP PN	0.30

RECOMMENDED OPERATING CONDITIONS, V_{CC} = 1.8 V ±10%

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		1.62	1.8	1.98	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	High-level input voltage		1.4		1.98	V
V_{IL}	Low-level input voltage		–0.3		0.4	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	All outputs			0.5	mA
I_{OL}	Low-level output current	All outputs			1	mA
	Oscillator/clock speed				16	MHz

RECOMMENDED OPERATING CONDITIONS, V_{CC} = 2.5 V ±10%

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.25	2.5	2.75	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	High-level input voltage		1.8		2.75	V
V_{IL}	Low-level input voltage		–0.3		0.6	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	All outputs			1	mA
I_{OL}	Low-level output current	All outputs			2	mA
	Oscillator/clock speed				16	MHz

RECOMMENDED OPERATING CONDITIONS, V_{CC} = 3.3 V ±10%

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_I	Input voltage		0		V_{CC}	V
V_{IH}	High-level input voltage		$0.7 \times V_{CC}$			V
V_{IL}	Low-level input voltage				$0.3 \times V_{CC}$	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	All outputs			1.8	mA
I_{OL}	Low-level output current	All outputs			3.2	mA
	Oscillator/clock speed				32	MHz

RECOMMENDED OPERATING CONDITIONS, V_{CC} = 5 V ±10%

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage				5.5	V
V_I	Input voltage				V_{CC}	V
V_{IH}	High-level input voltage	Except XIN	0			V
		XIN	$0.7 \times V_{CC}$			
V_{IL}	Low-level input voltage	Except XIN			0.8	V
		XIN			$0.3 \times V_{CC}$	
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	All outputs			4	mA
I_{OL}	Low-level output current	All outputs			4	mA
	Oscillator/clock speed				48	MHz

ELECTRICAL CHARACTERISTICS, V_{CC} = 1.8 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –0.5 mA		1.3			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA				0.5	V
I_I	Input current	V_{CC} = 1.98 V, V_I = 0 to 1.98 V,	V_{SS} = 0, All other terminals floating			10	µA
I_{OZ}	High-impedance state output current	V_{CC} = 1.98 V, V_O = 0 to 1.98 V, Chip selected in write mode or chip deselect	V_{SS} = 0,			±20	µA
I_{CC}	Supply current	V_{CC} = 1.98 V, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.4 V, No load on outputs,	T_A = 0°C, XTAL1 at 16 MHz, Baud rate = 1 Mbit/s			4.5	mA
$C_{I(CLK)}$	Clock input capacitance	V_{CC} = 0, f = 1 MHz, All other terminals grounded	V_{SS} = 0, T_A = 25°C,		5	7	pF
$C_{O(CLK)}$	Clock output capacitance				5	7	pF
C_I	Input capacitance				6	10	pF
C_O	Output capacitance				10	15	pF

ELECTRICAL CHARACTERISTICS, V_{CC} = 2.5 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA		1.8			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA				0.5	V
I_I	Input current	V_{CC} = 2.75 V, V_I = 0 to 2.75 V,	V_{SS} = 0, All other terminals floating			10	µA
I_{OZ}	High-impedance state output current	V_{CC} = 2.75 V, V_O = 0 to 2.75 V, Chip selected in write mode or chip deselect	V_{SS} = 0,			±20	µA
I_{CC}	Supply current	V_{CC} = 2.75 V, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.6 V, No load on outputs,	T_A = 0°C, XTAL1 at 24 MHz, Baud rate = 1.5 Mbit/s			90	mA
$C_{I(CLK)}$	Clock input capacitance	V_{CC} = 0, f = 1 MHz, All other terminals grounded	V_{SS} = 0, T_A = 25°C,		5	7	pF
$C_{O(CLK)}$	Clock output capacitance				5	7	pF
C_I	Input capacitance				6	10	pF
C_O	Output capacitance				10	15	pF

ELECTRICAL CHARACTERISTICS, V_{CC} = 3.3 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1.8 mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 3.2 mA				0.5	V
I_I	Input current	V_{CC} = 3.6 V, V_I = 0 to 3.6 V,	V_{SS} = 0, All other terminals floating			10	µA
I_{OZ}	High-impedance state output current	V_{CC} = 3.6 V, V_O = 0 to 3.6 V, Chip selected in write mode or chip deselect	V_{SS} = 0,			±20	µA
I_{CC}	Supply current	V_{CC} = 3.6 V, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, No load on outputs,	T_A = 0°C, XTAL1 at 32 MHz, Baud rate = 2 Mbit/s			16	mA
$C_{I(CLK)}$	Clock input capacitance	V_{CC} = 0, f = 1 MHz, All other terminals grounded	V_{SS} = 0, T_A = 25°C,		5	7	pF
$C_{O(CLK)}$	Clock output capacitance				5	7	pF
C_I	Input capacitance				6	10	pF
C_O	Output capacitance				10	15	pF

ELECTRICAL CHARACTERISTICS, V_{CC} = 5 V

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA		4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA				0.4	V
I_I	Input current	V_{CC} = 5.5 V, V_I = 0 to 5.5 V,	V_{SS} = 0, All other terminals floating			10	µA
I_{OZ}	High-impedance state output current	V_{CC} = 5.5 V, V_O = 0 to 5.5 V, Chip selected in write mode or chip deselect	V_{SS} = 0,			±20	µA
I_{CC}	Supply current	V_{CC} = 5.5 V, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, and $\overline{RI}$ at 2 V, All other inputs at 0.8 V, No load on outputs,	T_A = 0°C, XTAL1 at 48 MHz, Baud rate = 3 Mbit/s			40	mA
$C_{I(CLK)}$	Clock input capacitance	V_{CC} = 0, f = 1 MHz, All other terminals grounded	V_{SS} = 0, T_A = 25°C,		5	7	pF
$C_{O(CLK)}$	Clock output capacitance				5	7	pF
C_I	Input capacitance				6	10	pF
C_O	Output capacitance				10	15	pF

TYPICAL CHARACTERISTICS

All channels active

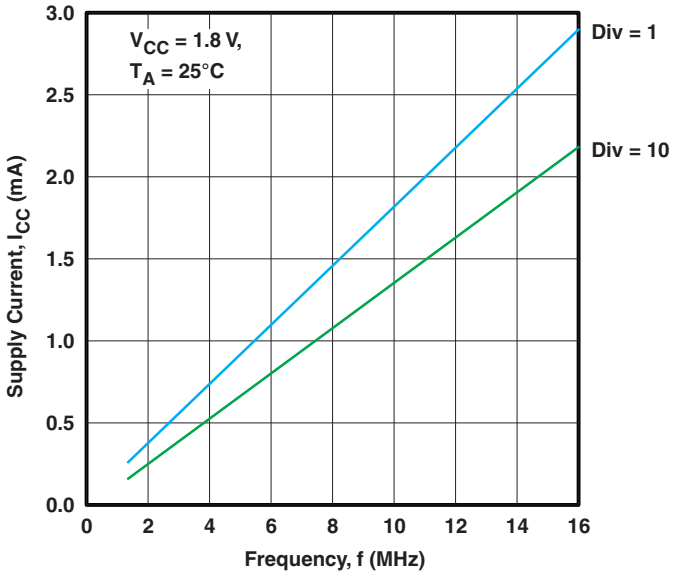


Figure 11. Supply Current vs Frequency (V_{CC} = 1.8 V)

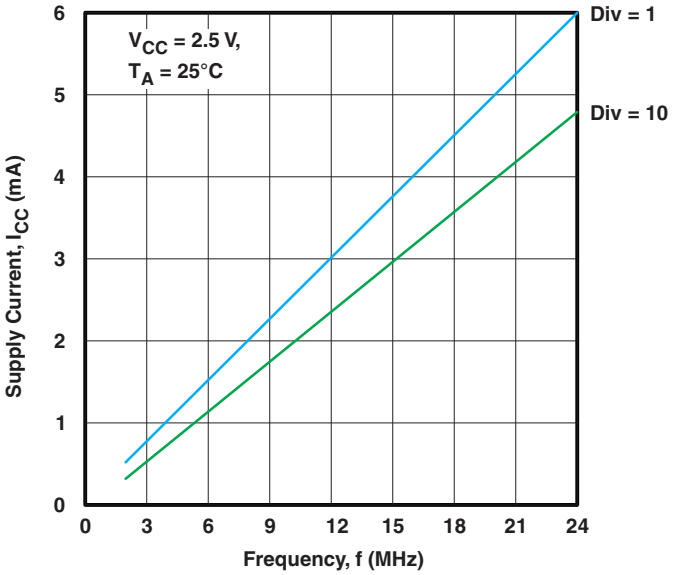


Figure 12. Supply Current vs Frequency (V_{CC} = 2.5 V)

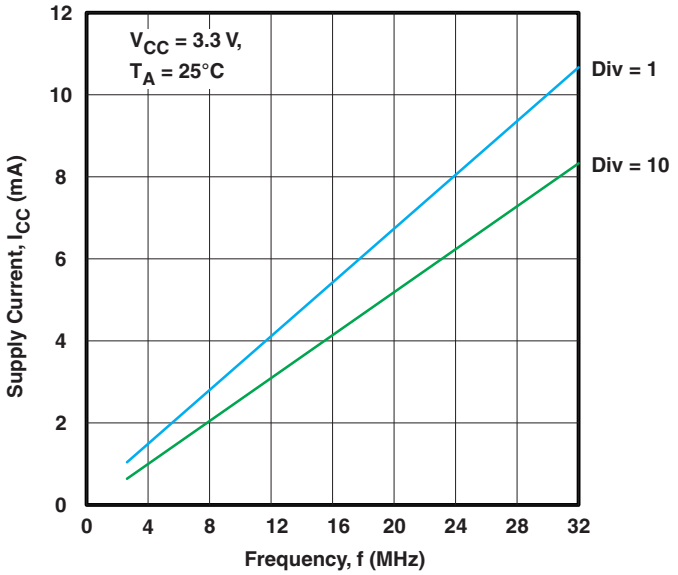


Figure 13. Supply Current vs Frequency (V_{CC} = 3.3 V)

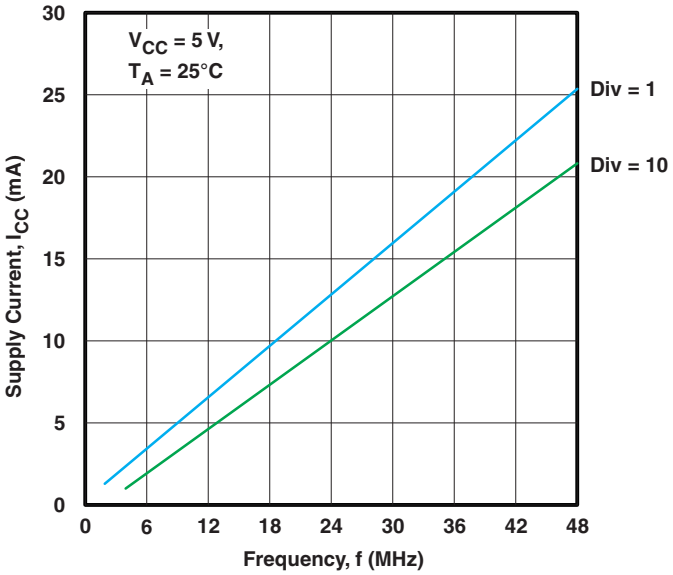


Figure 14. Supply Current vs Frequency (V_{CC} = 5 V)

TIMING REQUIREMENTS

T_A = 0°C to 70°C, V_{CC} = 1.8 V to 5 V ±10% (unless otherwise noted)

PARAMETER		TEST CONDITIONS	LIMITS								UNIT
			1.8 V		2.5 V		3.3 V		5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RESET}	Reset pulse width		200		200		200		200		ns
C_P	CP Clock period		63		42		32		20		ns
t_{3w}	Oscillator/Clock speed			16		24		32		48	MHz
t_{6s}	Address setup time		20		15		10		5		ns
t_{6h}	Address hold time	See Figure 15 and Figure 16	15		10		7		5		ns
t_{7w}	IOR strobe width	See Figure 15 and Figure 16	85		70		50		40		ns
t_{9d}	Read cycle delay	See Figure 16	85		70		60		50		ns
t_{12d}	Delay from IOR to data	See Figure 16		65		50		35		25	ns
t_{12h}	Data disable time			35		25		20		15	ns
t_{13w}	IOW strobe width	See Figure 15	85		70		50		40		ns
t_{15d}	Write cycle delay	See Figure 15	85		70		60		50		ns
t_{16s}	Data setup time	See Figure 15	40		30		20		15		ns
t_{16h}	Data hold time	See Figure 15	35		25		15		10		ns
t_{17d}	Delay from IOW to output	50 pF load, See Figure 17		60		40		30		20	ns
t_{18d}	Delay to set interrupt from MODEM input	50 pF load, See Figure 17		70		55		45		35	ns
t_{19d}	Delay to reset interrupt from IOR	50 pF load		80		55		40		30	ns
t_{20d}	Delay from stop to set interrupt	See Figure 18		1		1		1		1	Baudrate
t_{21d}	Delay from IOR to reset interrupt	50 pF load, See Figure 18		55		45		35		25	ns
t_{22d}	Delay from stop to interrupt	See Figure 21		1		1		1		1	Baudrate
t_{23d}	Delay from initial IOW reset to transmit star	See Figure 21	8	24	8	24	8	24	8	24	Baudrate
t_{24d}	Delay from IOW to reset interrupt	See Figure 21		75		45		35		25	ns
t_{25d}	Delay from stop to set RXRDY	See Figure 19 and Figure 20		1		1		1		1	Baudrate
t_{26d}	Delay from IOR to reset RXRDY	See Figure 19 and Figure 20		1		1		1		1	µs
t_{27d}	Delay from IOW to set TXRDY	See Figure 22 and Figure 23		70		60		50		40	ns
t_{28d}	Delay from start to reset TXRDY	See Figure 22 and Figure 23		16		16		16		16	Baudrate

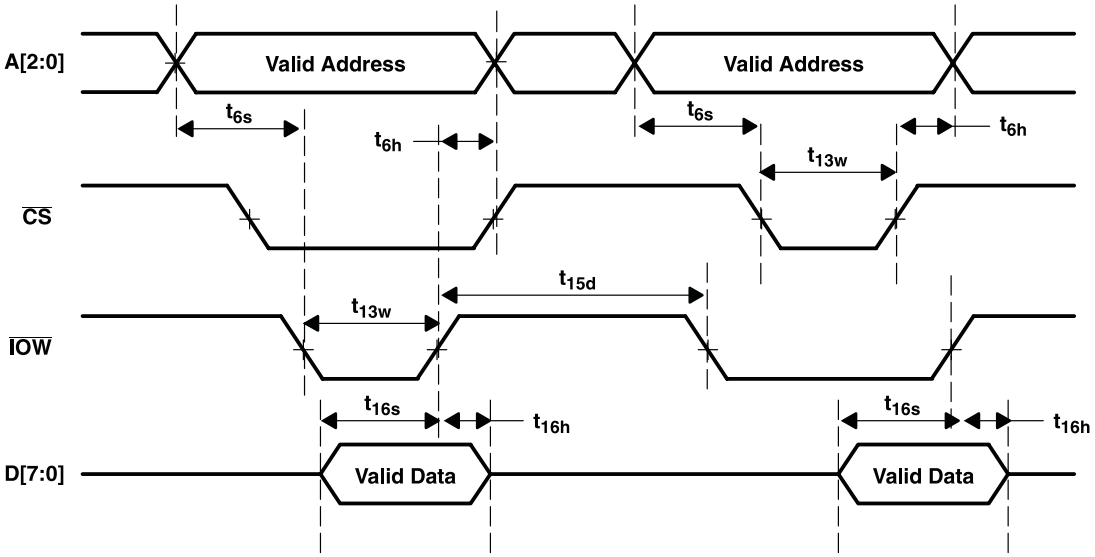


Figure 15. General Write Timing

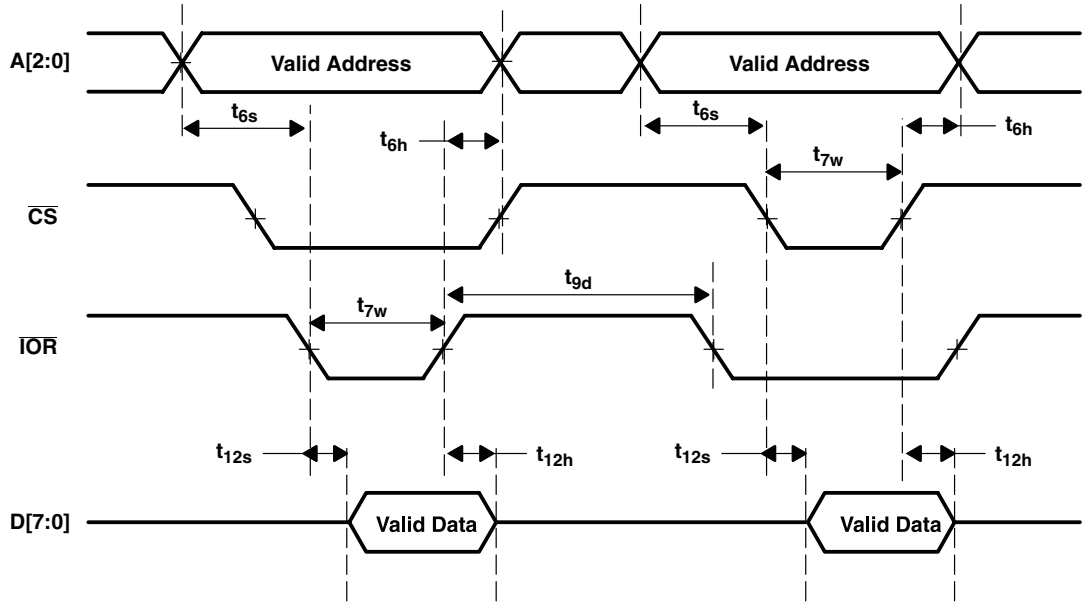


Figure 16. General Read Timing

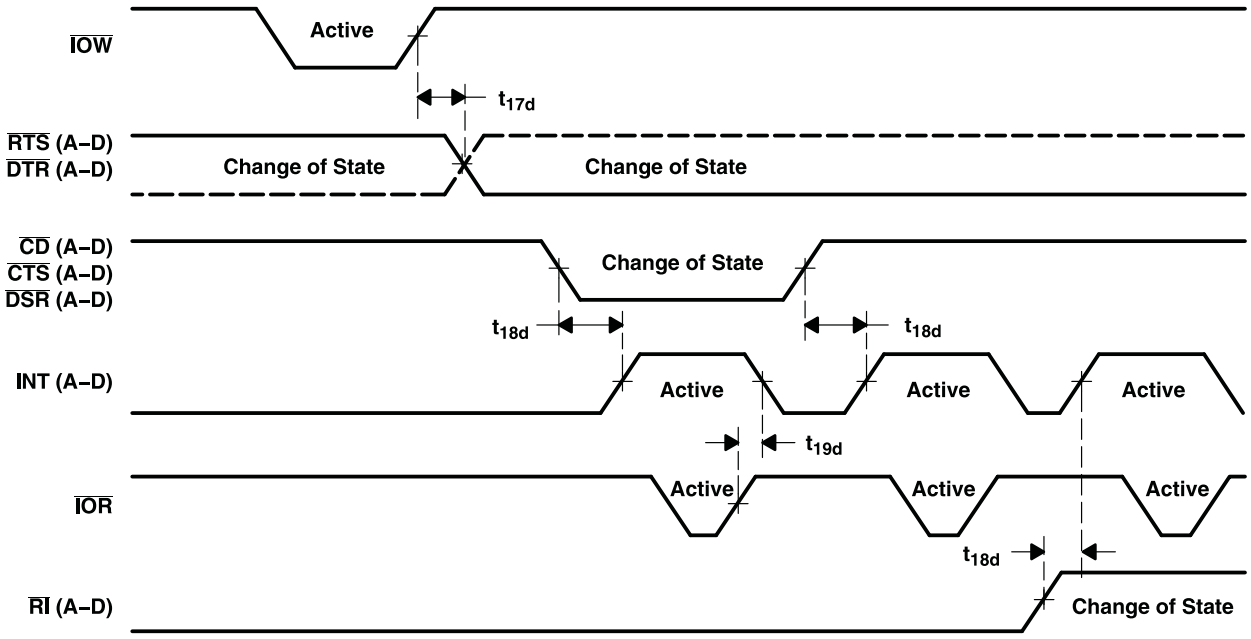


Figure 17. Modem/Output Timing

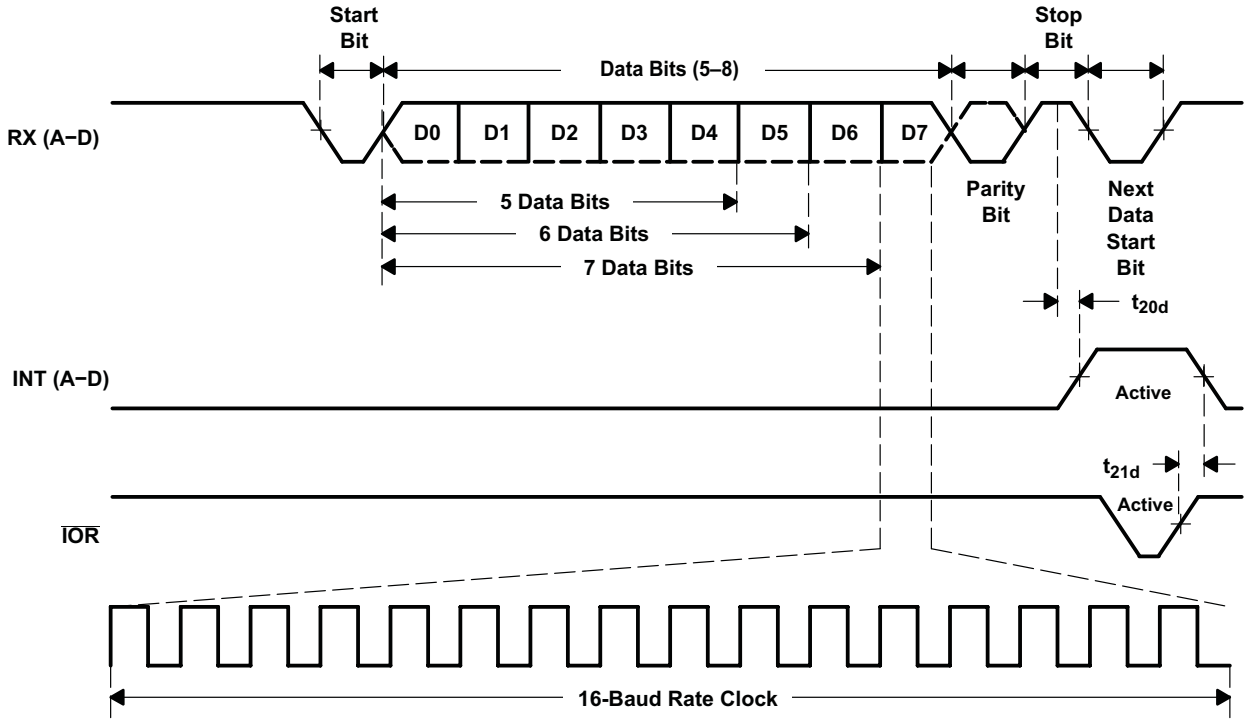


Figure 18. Receive Timing

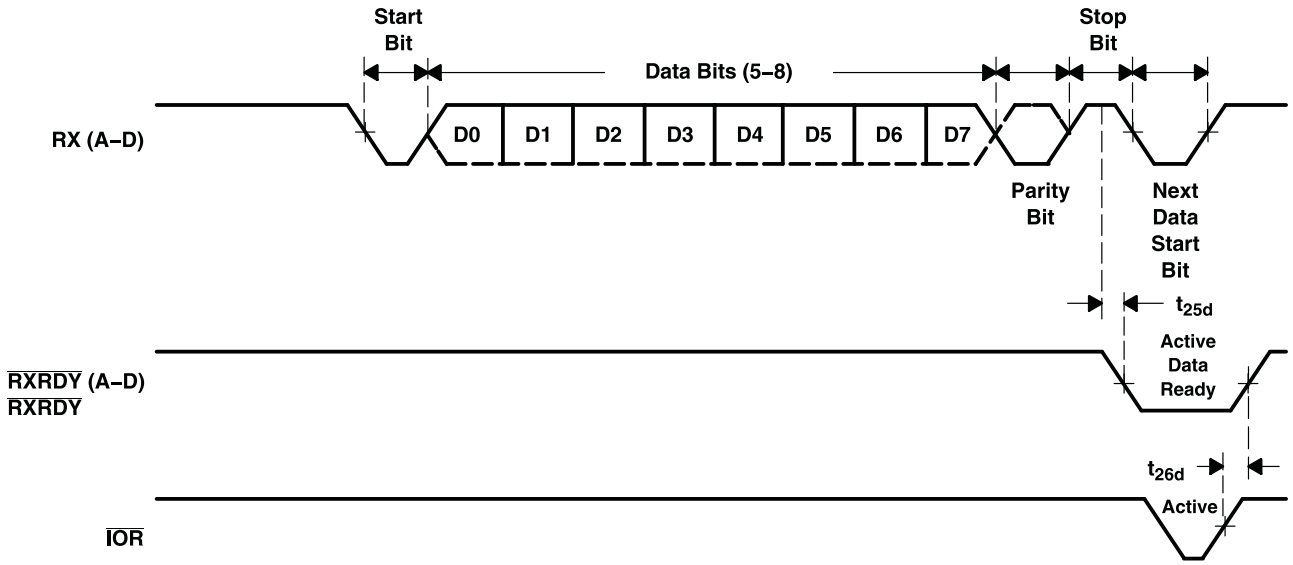


Figure 19. Receive Ready Timing in None FIFO Mode

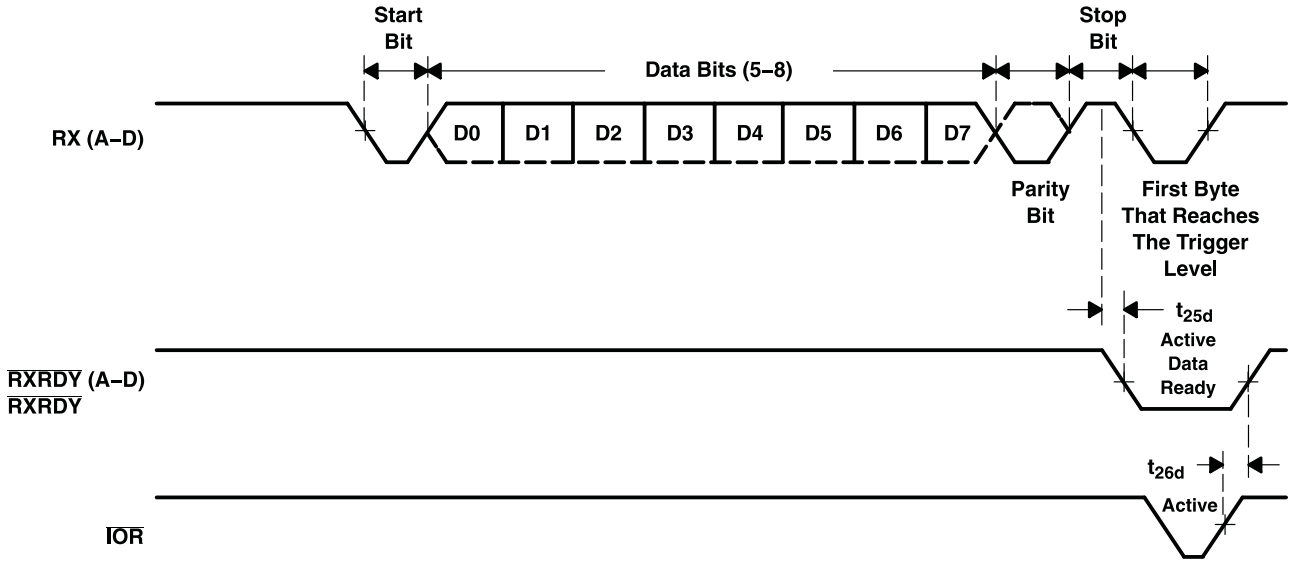


Figure 20. Receive Timing in FIFO Mode

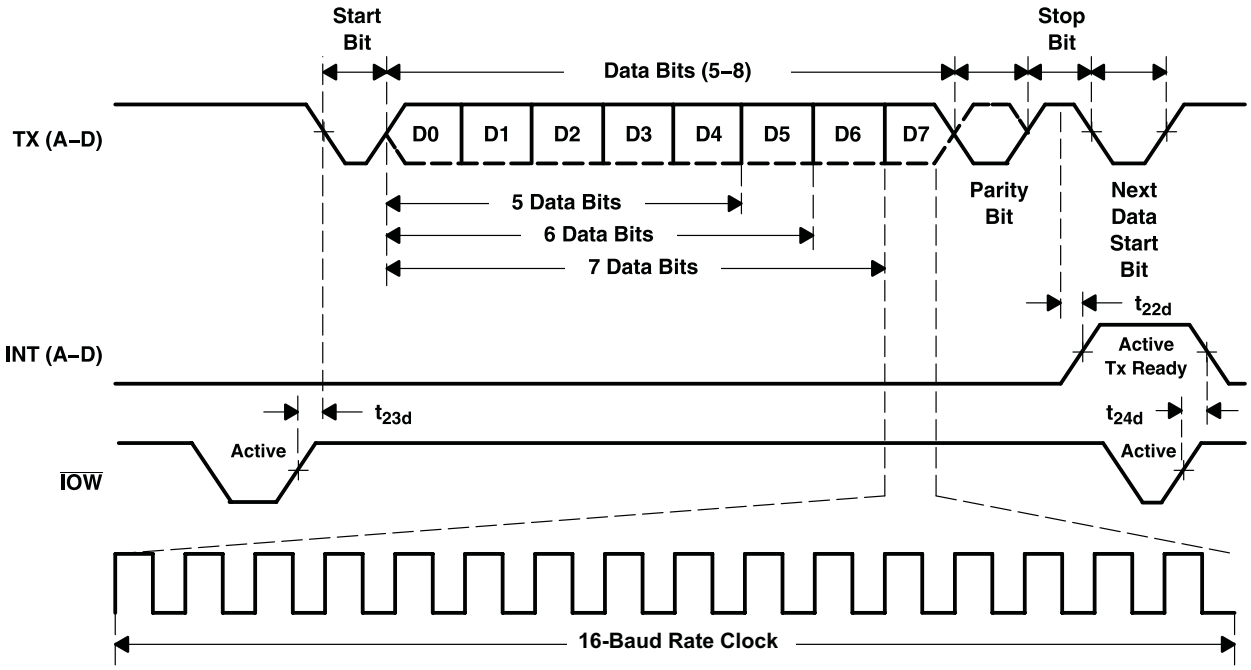


Figure 21. Transmit Timing

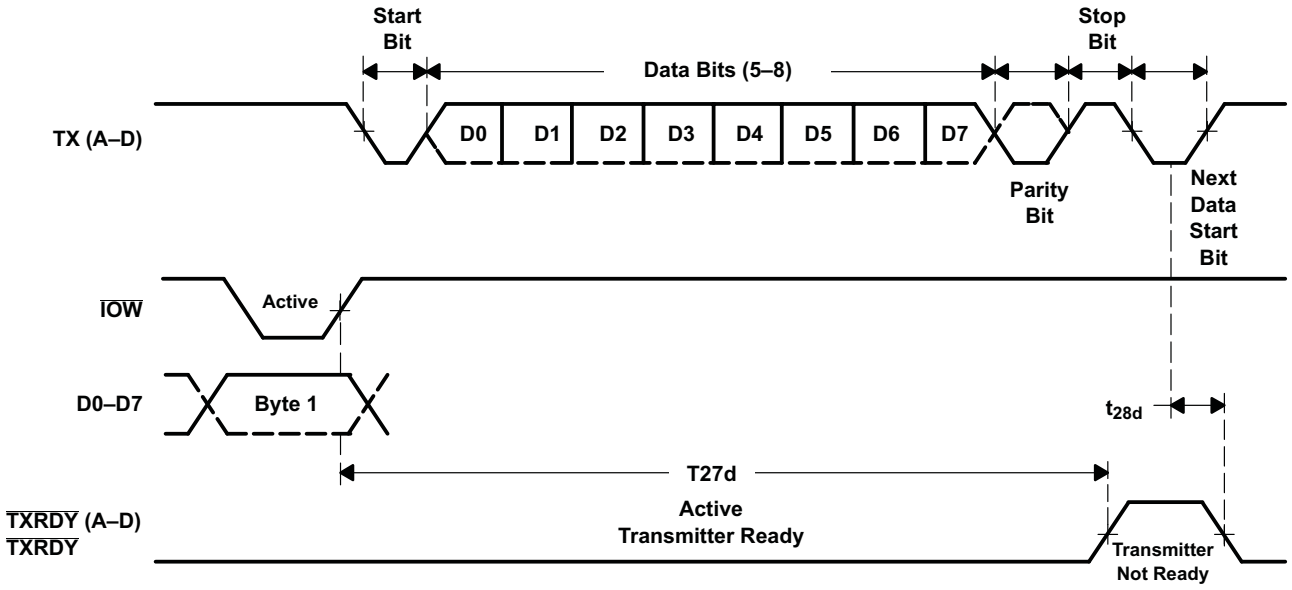


Figure 22. Transmit Ready Timing in None FIFO Mode

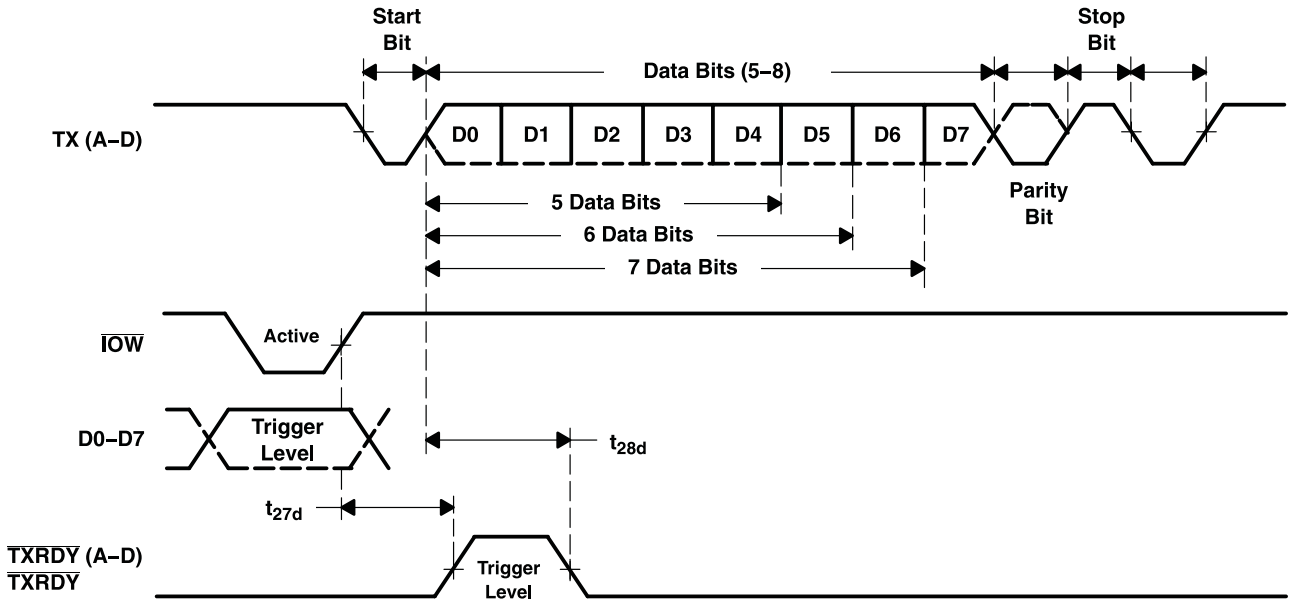


Figure 23. Transmit Timing in FIFO Mode

PRINCIPLES OF OPERATION

Register Map

Each register is selected using address lines A[0], A[1], A[2] and, in some cases, bits from other registers. The programming combinations for register selection are shown in Table 7.

Table 7. Register Map – Read/Write Properties(1)

A[2]	A[1]	A[0]	READ MODE	WRITE MODE
0	0	0	Receive holding register (RHR)	Transmit holding register (THR)
0	0	1	Interrupt enable register (IER)	Interrupt enable register
0	1	0	Interrupt identification register (IIR)	FIFO control register (FCR)
0	1	1	Line control register (LCR)	Line control register
1	0	0	Modem control register (MCR)	Modem control register
1	0	1	Line status register (LSR)	
1	1	0	Modem status register (MSR)	
1	1	1	Scratch register (SPR)	Scratch register (SPR)
0	0	0	Divisor latch LSB (DLL)	Divisor latch LSB (DLL)
0	0	1	Divisor latch MSB (DLH)	Divisor latch MSB (DLH)
1	0	0	Alternate function register (AFR)	Alternate function register (AFR)
0	1	0	Enhanced feature register (EFR)	Enhanced feature register
1	0	0	Xon-1 word	Xon-1 word
1	0	1	Xon-2 word	Xon-2 word
1	1	0	Xoff-1 word	Xoff-1 word
1	1	1	Xoff-2 word	Xoff-2 word
1	1	0	Transmission control register (TCR)	Transmission control register
1	1	1	Trigger level register (TLR)	Trigger level register
1	1	1	FIFO ready register	

(1) DLL and DLH are accessible only when LCR bit 7 is 1, and AFR is only accessible when LCR[7:5] = 100.
Enhanced feature register, Xon1, 2 and Xoff1, 2 are accessible only when LCR is set to 10111111 (8hBF).
Transmission control register and trigger level register are accessible only when EFR[4] = 1 and MCR[6] = 1, i.e. EFR[4] and MCR[6] are read/write enables.
FCR FIFORdy register is accessible when any CS A–D = 0, MCR[2] = 1 and loopback MCR [4] = 0 is disabled.
MCR[7] can only be modified when EFR[4] is set.

Table 8 lists and describes the '754C internal registers.

Table 8. '754C Internal Registers(1)(2)

SPECIAL CONSIDERATIONS	ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	READ/ WRITE
LCR[7] = 0	000	RHR	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit1	bit 0	Read
	000	THR	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit1	bit 0	Write
	001	IER	$\overline{CTS}$ interrupt enable	$\overline{RTS}$ interrupt enable	Xoff interrupt enable	Sleep mode	Modem status interrupt	Rx line status interrupt	THR empty interrupt	Rx data available interrupt	Read/ write
	010	FCR	Rx trigger level	Rx trigger level	TX trigger level	TX trigger level	DMA mode select	Resets Tx FIFO	Resets Rx FIFO	Enables FIFOs	Write
	010	IIR	FCR(0)	FCR(0)	$\overline{CTS}$, $\overline{RTS}$	Xoff	Interrupt priority Bit 2	Interrupt priority Bit 1	Interrupt priority Bit 0	Interrupt status	Read
None	011	LCR	DLAB and EFR enable	Break control bit	Sets parity	Parity type select	Parity enable	No. of stop bits	Word length	Word length	Read/ write
LCR[7:0] ≠ 1011 1111	100	MCR	1× or 4× clock	TCR and TLR enable	Xon any	Enable loopback	IRQ enable	FIFORdy Enable	$\overline{RTS}$	$\overline{DTR}$	Read/ write
	101	LSR	Error in Rx FIFO	THR and TSR empty	THR empty	Break interrupt	Framing error	Parity error	Overrun error	Data in receiver	Read
	110	MSR	$\overline{CD}$	$\overline{RI}$	$\overline{DSR}$	$\overline{CTS}$	Δ$\overline{CD}$	Δ$\overline{RI}$	Δ$\overline{DSR}$	Δ$\overline{CTS}$	Read
	111	SPR	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit1	bit 0	Read/ write
LCR[7] = 1	000	DLL	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit1	bit 0	Read/ write
	001	DLH	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	Read/ write
LCR[7:0] = 100	010	AFR	DLY2	DLY1	DLY0	RCVEN	485LG	485RN	IREN	CONC	Read/ write
LCR[7:0] = 1011 1111	010	EFR	Auto-$\overline{CTS}$	Auto-$\overline{RTS}$	Special character detect	Enable enhanced-functions	S/W flow control Bit 3	S/W flow control Bit 2	S/W flow control Bit 1	S/W flow control Bit 0	Read/ write
	100	Xon1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit1	bit 0	Read/ write
	101	Xon2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit1	bit 0	Read/ write
	110	Xoff1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit1	bit 0	Read/ write
	111	Xoff2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit1	bit 0	Read/ write
EFR[4] = 1 and MCR[6] = 1	110	TCR	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit1	bit 0	Read/ write
	111	TLR	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit1	bit 0	Read/ write
MCR[4] = 0 and MCR[2] = 1	111	FIFORdy	RX FIFO D status	RX FIFO C status	RX FIFO B status	RX FIFO A status	TX FIFO D status	TX FIFO C status	TX FIFO B status	TX FIFO A status	Read

(1) Bits represented by shaded cells can only be modified if EFR[4] is enabled, i.e., if enhanced functions are enabled.
(2) Refer to the notes under Table 7 for more register access information.

Receiver Holding Register (RHR)

The receiver section consists of the receiver holding register (RHR) and the receiver shift register (RSR). The RHR is actually a 64-byte FIFO. The RSR receives serial data from RX terminal. The data is converted to parallel data and moved to the RHR. The receiver section is controlled by the line control register. If the FIFO is disabled, location zero of the FIFO is used to store the characters. If overflow occurs, characters are lost. The RHR also stores the error status bits associated with each character.

Transmit Holding Register (THR)

The transmitter section consists of the transmit holding register (THR) and the transmit shift register (TSR). The transmit holding register is actually a 64-byte FIFO. The THR receives data and shifts it into the TSR where it is converted to serial data and moved out on the TX terminal. If the FIFO is disabled, location zero of the FIFO is used to store the byte. Characters are lost if overflow occurs.

FIFO Control Register (FCR)

This is a write-only register which is used for enabling the FIFOs, clearing the FIFOs, setting transmitter and receiver trigger levels, and selecting the type of DMA Signaling. Table 9 shows FIFO control register bit settings.

Table 9. FIFO Control Register (FCR) Bit Settings

BIT NO.	BIT SETTINGS
0	0 = Disable the transmit and receive FIFOs 1 = Enable the transmit and receive FIFOs
1	0 = No change 1 = Clears the receive FIFO and resets it's counter logic to zero. Will return to zero after clearing FIFO.
2	0 = No change 1 = Clears the transmit FIFO and resets it's counter logic to zero. Will return to zero after clearing FIFO.
3	0 = DMA Mode 0 1 = DMA Mode 1
5:4 (1)	Sets the trigger level for the TX FIFO: 00 – 8 spaces 01 – 16 spaces 10 – 32 spaces 11 – 56 spaces
7:6	Sets the trigger level for the RX FIFO: 00 – 1 characters 01 – 4 characters 10 – 56 characters 11 – 60 characters

(1) FCR[5−4] can be modified and enabled only when EFR[4] is set. This is because the transmit trigger level is regarded as an enhanced function.

Line Control Register (LCR)

This register controls the data communication format. The word length, number of stop bits, and parity type are selected by writing the appropriate bits to the LCR. Table 10 shows line control register bit settings.

Table 10. Line Control Register (LCR) Bit Settings

BIT NO.	BIT SETTINGS
1:0	Specifies the word length to be transmitted or received. 00 – 5 bits 01 – 6 bits 10 − 7 bits 11 – 8 bits
2	Specifies the number of stop bits: 0 – 1 stop bits (Word length = 5, 6, 7, 8) 1 – 1.5 stop bits (Word length = 5) 1 – 2 stop bits (Word length = 6, 7, 8) 3
3	0 = No parity 1 = A parity bit is generated during transmission and the receiver checks for received parity.
4	0 = Odd parity is generated (if LCR[3] = 1) 1 = Even parity is generated (if LCR[3] = 1)
5	Selects the forced parity format (if LCR(3) = 1) If LCR[5] = 1 and LCR[4] = 0 the parity bit is forced to 1 in the transmitted and received data. If LCR[5] = 1 and LCR[4] = 1 the parity bit is forced to 0 in the transmitted and received data.
6	Break control bit. 0 = Normal operating condition 1 = Forces the transmitter output to go low to alert the communication terminal.
7	0 = Normal operating condition 1 = Divisor latch enable

Line Status Register (LSR)

Table 11 shows line status register bit settings.

Table 11. Line Status Register (LSR) Bit Settings

BIT NO.	BIT SETTINGS
0	0 = No data in the receive FIFO 1 = At least one character in the RX FIFO
1	0 = No overrun error 1 = Overrun error has occurred.
2	0 = No parity error in data being read from RX FIFO 1 = Parity error in data being read from RX FIFO
3	0 = No framing error in data being read from RX FIFO 1 = Framing error occurred in data being read from RX FIFO (i.e., received data did not have a valid stop bit)
4	0 = No break condition 1 = A break condition occurred and associated byte is 00. (i.e., RX was low for at least one character time frame).
5	0 = Transmit hold register is NOT empty 1 = Transmit hold register is empty. The processor can now load up to 64 bytes of data into the THR if the TX FIFO is enabled.
6	0 = Transmitter hold AND shift registers are not empty. 1 = Transmitter hold AND shift registers are empty.
7	0 = Normal operation 1 = At least one parity error, framing error or break indication are stored in the receiver FIFO. Bit 7 is cleared when no errors are present in the FIFO.

When the LSR is read, LSR[4:2] reflects the error bits [BI, FE, PE] of the character at the top of the RX FIFO (next character to be read). The LSR[4:2] registers do not physically exist, as the data read from the RX FIFO is output directly onto the output data-bus, DI[4:2], when the LSR is read. Therefore, errors in a character are identified by reading the LSR and then reading the RHR.

LSR[7] is set when there is an error anywhere in the RX FIFO and is cleared only when there are no more errors remaining in the FIFO.

NOTE:

Reading the LSR does not cause an increment of the RX FIFO read pointer. The RX FIFO read pointer is incremented by reading the RHR.

Modem Control Register (MCR)

The MCR controls the interface with the modem, data set, or peripheral device that is emulating the modem. Table 12 shows modem control register bit settings.

Table 12. Modem Control Register (MCR) Bit Settings(1)

BIT NO.	BIT SETTINGS
0	0 = Force $\overline{\text{DTR}}$ output to inactive (high) 1 = Force $\overline{\text{DTR}}$ output to active (low). In loopback controls MSR[5].
1	0 = Force $\overline{\text{RTS}}$ output to inactive (high) 1 = Force $\overline{\text{RTS}}$ output to active (low). In loopback controls MSR[4]. If Auto-$\overline{\text{RTS}}$ is enabled the $\overline{\text{RTS}}$ output is controlled by hardware flow control
2	0 Disables the FIFORdy register 1 Enable the FIFORdy register. In loopback controls MSR[6].
3	0 = Forces the IRQ(A–D) outputs to high-impedance state 1 = Forces the IRQ(A–D) outputs to the active state. In loopback controls MSR[7].
4	0 = Normal operating mode 1 = Enable local loopback mode (internal) In this mode the MCR[3:0] signals are looped back into MSR[3:0] and the TX output is looped back to the RX input internally.
5	0 = Disable Xon Any function 1 = Enable Xon Any function
6	0 = No action 1 = Enable access to the TCR and TLR registers.
7	0 = Divide by one clock input 1 = Divide by four clock input This bit reflects the inverse of the CLKSEL pin value at the trailing edge of the RESET pulse.

(1) MCR[7:5] can only be modified when EFR[4] is set i.e., EFR[4] is a write enable.

Modem Status Register (MSR)

This 8-bit register provides information about the current state of the control lines from the modem, data set, or peripheral device to the processor. It also indicates when a control input from the modem changes state. Table 13 shows modem status register bit settings.

Table 13. Modem Status Register (MSR) Bit Settings(1)

BIT NO.	BIT SETTINGS
0	Indicates that $\overline{CTS}$ input (or MCR[1] in loopback) has changed state. Cleared on a read.
1	Indicates that $\overline{DSR}$ input (or MCR[0] in loopback) has changed state. Cleared on a read.
2	Indicates that $\overline{RI}$ input (or MCR[2] in loopback) has changed state from low to high. Cleared on a read.
3	Indicates that $\overline{CD}$ input (or MCR[3] in loopback) has changed state. Cleared on a read.
4	This bit is equivalent to MCR[1] during local loop-back mode. It is the complement to the $\overline{CTS}$ input.
5	This bit is equivalent to MCR[0] during local loop-back mode. It is the complement to the $\overline{DSR}$ input.
6	This bit is equivalent to MCR[2] during local loop-back mode. It is the complement to the $\overline{RI}$ input.
7	This bit is equivalent to MCR[3] during local loop-back mode. It is the complement to the $\overline{CD}$ input.

(1) The primary inputs $\overline{RI}$, $\overline{CD}$, $\overline{CTS}$, $\overline{DSR}$ are all active low but their registered equivalents in the MSR and MCR (in loopback) registers are active high.

Interrupt Enable Register (IER)

The interrupt enable register (IER) enables each of the six types of interrupt, receiver error, RHR interrupt, THR interrupt, Xoff received, or $\overline{CTS}$/$\overline{RTS}$ change of state from low to high. The INT output signal is activated in response to interrupt generation. Table 14 shows interrupt enable register bit settings.

Table 14. Interrupt Enable Register (IER) Bit Settings(1)

BIT NO.	BIT SETTINGS
0	0 = Disable the RHR interrupt 1 = Enable the RHR interrupt
1	0 = Disable the THR interrupt 1 = Enable the THR interrupt
2	0 = Disable the receiver line status interrupt 1 = Enable the receiver line status interrupt
3	0 = Disable the modem status register interrupt 1 = Enable the modem status register interrupt
4	0 = Disable sleep mode 1 = Enable sleep mode
5	0 = Disable the Xoff interrupt 1 = Enable the Xoff interrupt
6	0 = Disable the $\overline{RTS}$ interrupt 1 = Enable the $\overline{RTS}$ interrupt
7	0 = Disable the $\overline{CTS}$ interrupt 1 = Enable the $\overline{CTS}$ interrupt

(1) IER[7:4] can only be modified if EFR[4] is set, i.e., EFR[4] is a write enable.
Re-enabling IER[1] will cause a new interrupt, if the THR is below the threshold.

Interrupt Identification Register (IIR)

The IIR is a read-only 8-bit register which provides the source of the interrupt in a prioritized manner. Table 15 shows interrupt identification register bit settings.

Table 15. Interrupt Identification Register (IIR) Bit Settings

BIT NO.	BIT SETTINGS
0	0 = An interrupt is pending 1 = No interrupt is pending
3:1	3-Bit encoded interrupt. See Table 14.
4	1 = Xoff/Special character has been detected.
5	$\overline{CTS}$/$\overline{RTS}$ low to high change of state
7:6	Mirror the contents of FCR[0]

The interrupt priority list is illustrated in Table 16.

Table 16. Interrupt Priority List

PRIORITY LEVEL	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	INTERRUPT SOURCE
1	0	0	0	1	1	0	Receiver line status error
2	0	0	1	1	0	0	Receiver timeout interrupt
2	0	0	0	1	0	0	RHR interrupt
3	0	0	0	0	1	0	THR interrupt
4	0	0	1	0	0	0	Modem interrupt
5	0	1	0	0	0	0	Received Xoff signal/special character
6	1	0	0	0	0	0	$\overline{CTS}$, $\overline{RTS}$ change of state from active (low) to inactive (high)

Enhanced Feature Register (EFR)

This 8-bit register enables or disables the enhanced features of the UART. Table 17 shows the enhanced feature register bit settings.

Table 17. Enhanced Feature Register (EFR) Bit Settings

BIT NO.	BIT SETTINGS
3:0	Combinations of software flow control can be selected by programming bit 3−bit 0. See Table 1.
4	Enhanced functions enable bit. 0 = Disables enhanced functions and writing to IER[7:4], FCR[5:4], MCR[7:5]. 1 = Enables the enhanced function IER[7:4], FCR[5:4], and MCR[7:5] can be modified, i.e., this bit is therefore a write enable.
5	0 = Normal operation 1 = Special character detect. Received data is compared with Xoff-2 data. If a match occurs, the received data is transferred to FIFO and IIR[4] is set to 1 to indicate a special character has been detected.
6	$\overline{RTS}$ flow control enable bit 0 = Normal operation 1 = $\overline{RTS}$ flow control is enabled i.e., $\overline{RTS}$ pin goes high when the receiver FIFO HALT trigger level TCR[3:0] is reached, and goes low when the receiver FIFO RESTORE transmission trigger level TCR[7:4] is reached.
7	$\overline{CTS}$ flow control enable bit 0 = Normal operation 1 = $\overline{CTS}$ flow control is enabled i.e., transmission is halted when a high signal is detected on the $\overline{CTS}$ pin.

Divisor Latches (DLL, DLH)

Two 8-bit registers store the 16-bit divisor for generation of the baud clock in the baud rate generator. DLH, stores the most significant part of the divisor. DLL stores the least significant part of the division.

DLL and DLH can only be written to before sleep mode is enabled (i.e., before IER[4] is set).

Transmission Control Register (TCR)

This 8-bit register is used to store the receive FIFO threshold levels to start/stop transmission during hardware/software flow control. Table 18 shows transmission control register bit settings.

Table 18. Transmission Control Register (TCR) Bit Settings

BIT NO.	BIT SETTINGS
3:0	RCV FIFO trigger level to HALT transmission (0–60)
7:4	RCV FIFO trigger level to RESTORE transmission (0–60)

TCR trigger levels are available from 0–60 bytes with a granularity of four.

TCR can be written to only when EFR[4] = 1 and MCR[6] = 1. The programmer must program the TCR such that TCR[3:0] > TCR[7:4]. There is no built-in hardware check to make sure this condition is met. Also, the TCR must be programmed with this condition before Auto-$\overline{\text{RTS}}$ or software flow control is enabled to avoid spurious operation of the device.

Trigger Level Register (TLR)

This 8-bit register is used to store the transmit and received FIFO trigger levels used for DMA and interrupt generation. Trigger levels from 4−60 can be programmed with a granularity of 4. Table 19 shows trigger level register bit settings.

Table 19. Trigger Level Register (TLR) Bit Settings

BIT NO.	BIT SETTINGS
3:0	Transmit FIFO trigger levels (4–60), number of spaces available
7:4	RCV FIFO trigger levels (4–60), number of characters available

TLR can be written to only when EFR[4] = 1 and MCR[6] = 1. If TLR[3:0] or TLR[7:4] are zero, then the selectable trigger levels via the FIFO control register (FCR) are used for the transmit and receive FIFO trigger levels. Trigger levels from 4–60 bytes are available with a granularity of four. The TLR should be programmed for N/4, where N is the desired trigger level.

FIFO Ready Register

The FIFO ready register provides real-time status of the transmit and receive FIFOs. Table 20 shows the FIFO ready register bit settings.

Table 20. FIFO Ready Register

BIT NO.	BIT SETTINGS
3:0	0 = There are less than a TX trigger level number of spaces available in the TX FIFO. 1 = There are at least a TX trigger level number of spaces available in the TX FIFO
7:4	0 = There are less than a RX trigger level number of characters in the RX FIFO. 1 = The RX FIFO has more than a RX trigger level number of characters available for reading OR a timeout condition has occurred.

The FIFORdy register is a read only register and can be accessed when any of the four UARTs are selected CS A–D = 0, MCR[2] (FIFORdy Enable) is a 1 and loopback is disabled. Its address space is 111.

Alternate Function Register (AFR)

The alternate function register (AFR) is used to enable some extra functionality beyond the capabilities of the original TL16C754. The first of these is a concurrent write mode, which can be useful in more expediently setting up all four UART channels. The second addition is the IrDA mode, which supports Standard IrDA (SIR) mode with baud rates from 2400 to 115.2 bps. The third addition is support for RS-485 bus drivers or transceivers by providing an output pin ($\overline{\text{DTR}}$x) per channel, which is timed to keep the RS-485 driver enabled as long as transmit data is pending.

The AFR is located at A[2:0] = 010 when LCR[7:5] = 100.

Table 21. Transmission Control Register (TCR) Bit Settings

BIT NO.	BIT SETTINGS
0	CONC enables the concurrent write of all four (754) or two (752) channels simultaneously, which helps speed up initialization. Ensure that any indirect addressing modes have been enabled before using.
1	IREN enables the IrDA SIR mode. This mode is only specified to 115.2 bps and use of this mode at higher speeds is not recommended.
2	485EN enables the half duplex RS-485 mode and causes the $\overline{\text{DTR}}$x output to be set high whenever there is any data in the THR or TSR and to be held high until the delay set by DLY3:0 has expired, at which time it will be set low. The $\overline{\text{DTR}}$x output is intended to drive the enabled input of an RS-485 driver. When this bit is set, the transmitter interrupts will be held off until the TSR is empty, unless 485LG is set.
3	485LG is set when the 485EN is set. This bit indicates that a relatively large data block is being set, requiring more than a single load of the xmt fifo. In this case, the transmitter interrupts occur as in the standard RS-232 mode, either when the xmt fifo contents drop below the xmt threshold or when the xmt fifo is empty.
4	RCVEN is valid only when 485EN or IREN is set, and allows the serial receiver to listen in or snoop on the RS485 traffic or IrDA traffic. RS485 mode is generally considered half duplex, and usually a node is either driving or receiving, but there can be cases when it is advantageous to verify what you are sending. This can be used to detect collisions or as part of an arbitration mechanism on the bus. When both RCVEN and 485EN are set, the receiver will store any data presented on RX, if any. Note that implies that the external RS485 receiver is enabled. Whenever 485EN is cleared, the serial receiver is enabled for normal full duplex RS232 traffic. If RCVEN is cleared while 485EN is set, the receiver will be disabled. Standard IrDA (SIR) is also considered half duplex. Often the light energy from the transmitting LED is coupled back into the receiving PIN diode, which creates an input data stream that is not of interest to the host. Disabling the receiver (clearing RCVEN) prevents this reception, and eliminates the task of unloading the data. On the other hand, for diagnostic or other purposes, it may be useful to observe this data stream. For example, a mirror could be used to intentionally couple the output LED to the input PIN. For these cases, RCVEN could be set to enable the receiver. NOTE: When RCVEN is cleared (set to 0), the character timeout interrupt is not available, even in RSA-232 mode. This can be useful when checking code for valid threshold interrupts, as the timeout interrupt will not override the threshold interrupt.
7:5	DLY3–DLY0 sets a delay after the last stop bit of the last data byte being set before the $\overline{\text{DTR}}$x is set low, to allow for long cable runs. The delay is in number of bit times and is enabled by 485EN. The delay will start only when both the xmt serial shift register (TSR) is empty and the xmt fifo (THR) is empty, and if started, will be cleared by any data being written to the THR.

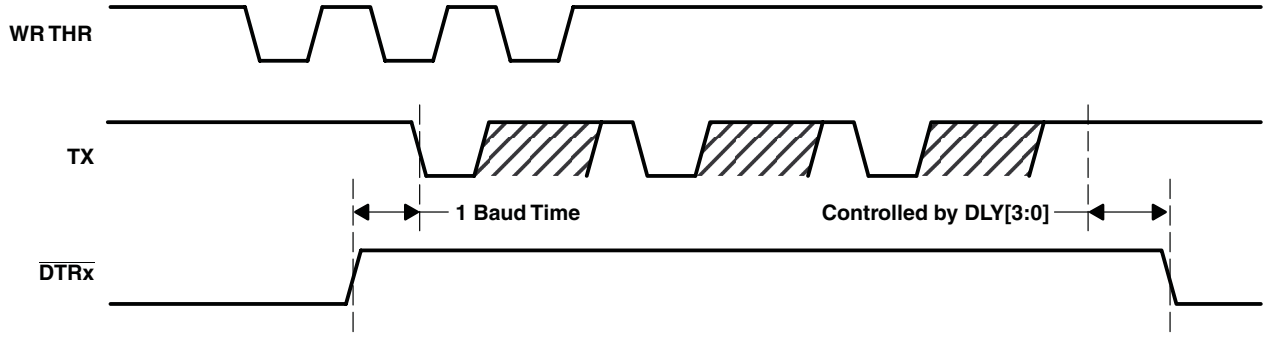
Table 22. LOOP and RCVEN Functionality

LOOP MODE	RCVEN	AFR	MODE	DESCRIPTION
LOOP mode off, MCR4 = 0, RX, TX active	RCVEN = 1	AFR = 10	RS-232	Receive threshold, timeout, and error detection interrupts available. Data stored in receive FIFO.
		AFR = 14	RS-485	Receive threshold, timeout, and error detection interrupts available. Data stored in receive FIFO.
		AFR = 12	IrDA	Receive threshold, timeout, and error detection interrupts available. Data stored in receive FIFO.
	RCVEN = 0	AFR = 00	RS-232	Receive threshold and error detection interrupts available. Data stored in receive FIFO.
		AFR = 04	RS-485	No data stored in receive FIFO, hence no interrupts available.
		AFR = 02	IrDA	No data stored in receive FIFO, hence no interrupts available.
LOOP mode on, MCR4 = 1, RX, TX inactive	RCVEN = 1	AFR = 10	RS-232	Receive threshold, timeout, and error detection interrupts available. Data stored in receive FIFO.
		AFR = 14	RS-485	Receive threshold, timeout, and error detection interrupts available. Data stored in receive FIFO.
		AFR = 12	IrDA	Receive threshold, timeout, and error detection interrupts available. Data stored in receive FIFO.
	RCVEN = 0	AFR = 00	RS-232	Receive threshold and error detection interrupts available. Data stored in receive FIFO.
		AFR = 04	RS-485	Receive threshold and error detection interrupts available. Data stored in receive FIFO.
		AFR = 02	IrDA	Receive threshold and error detection interrupts available. Data stored in receive FIFO.

RS-485 Mode

The RS-485 mode is intended to simplify the interface between the UART channel and an RS-485 driver or transceiver. When enabled by setting 485EN, the $\overline{\text{DTR}}$x output goes high one bit time before the first stop bit of the first data byte being sent, and remains high as long as there is pending data in the transmitter shift register (TSR) or transmitter holding register (THR, xmt fifo). Once both are empty (after the last stop bit of the last data byte), the $\overline{\text{DTR}}$x output stays high for a programmable delay of 0 to 15 bit times, as set by DLY[3:0]. This helps preserve data integrity over long signal lines. This is illustrated in the following.

Often RS-485 packets are relatively short and the entire packet can fit within the 64 byte xmt fifo. In this case, it goes empty when the TSR goes empty. But in cases where a larger block needs to be sent, it is advantageous to reload the xmt fifo as soon as it is depleted. Otherwise, the transmission stalls while waiting for the xmt fifo to be reloaded, which varies with processor load. In this case, it is best to also set 485LG (large block) which causes the transmit interrupt to occur wither when the THR becomes empty (if the xmt fifo level was not above the threshold), or when the xmt fifo threshold is crossed. The reloading of the xmt fifo occurs while some data is being shifted out, eliminating fifo underrun. If desired, when the last bytes of a current transmission are being loaded in the xmt fifo, 485LG can be cleared before the load and the transmit interrupt occurs on the TSR going empty.



A. Waveforms are not shown to scale, as the WR THR pulses typically are less than 100 ns, where the TX waveform varies with baud rate but is typically in the microsecond range.

Figure 24. $\overline{\text{DTRx}}$ and Transmit Data Relationship

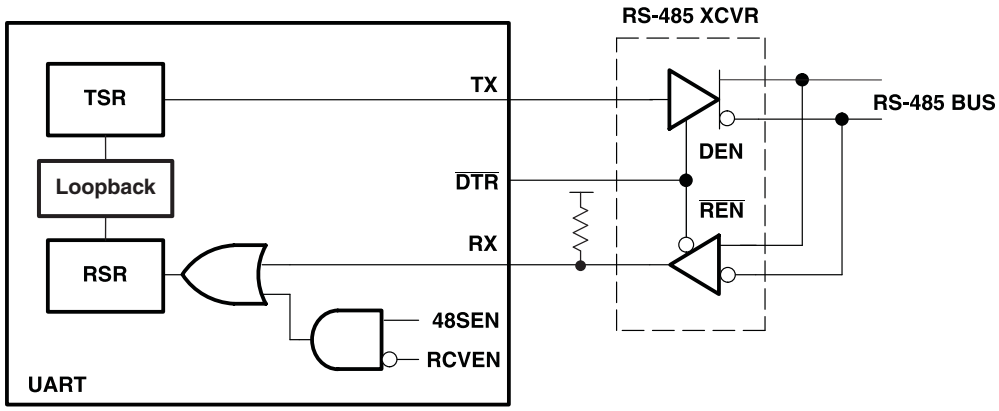


Figure 25. RS-485 Application Example 1

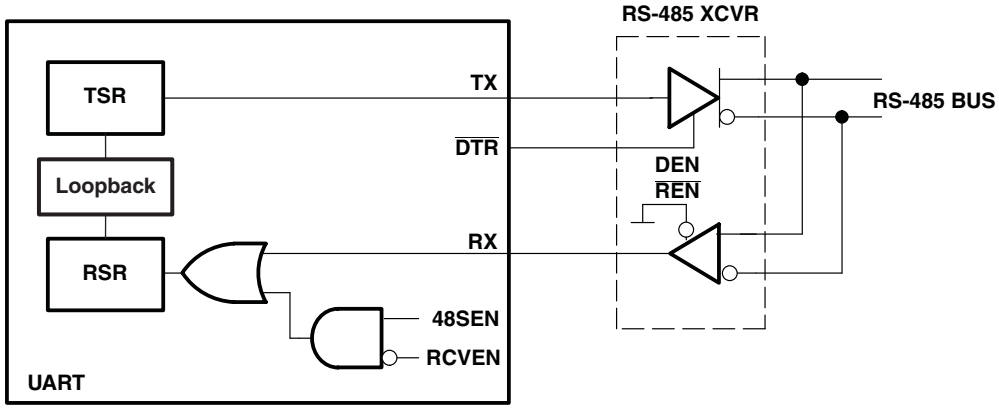


Figure 26. RS-485 Application Example 2

IrDA Overview

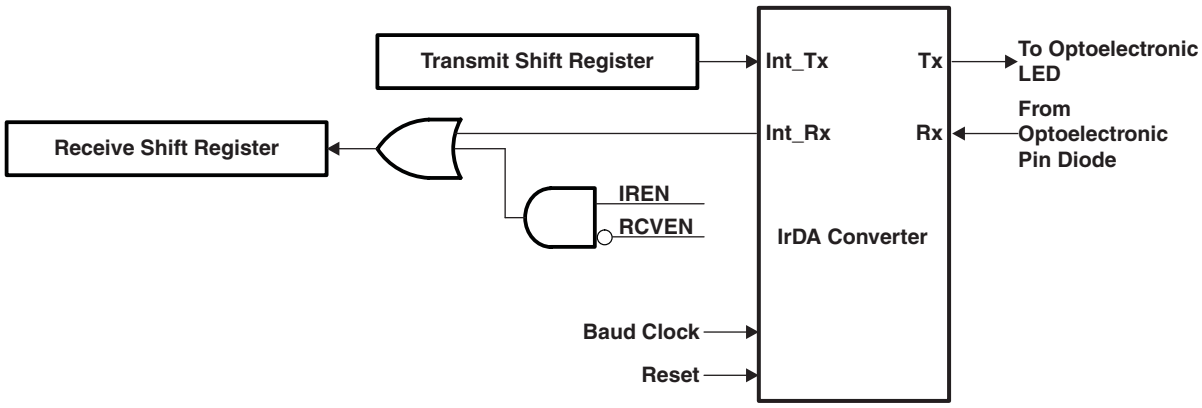


Figure 27. IrDA Mode

The infrared data association (IrDA) defines several protocols for sending and receiving serial infrared data, including rates of 115.2 kbps, 0.576 Mbps, 1.152 Mbps, and 4 Mbps. The low rate of 115.2 kbps was specified first and the others must maintain downward compatibility with it. At the 115.2 kbps rate, the protocol implemented in the hardware is fairly simple. It primarily defines a serial infrared data word to be surrounded by a start bit equal to 0 and a stop bit equal to 1. Individual bits are encoded or decoded the same whether they are

start, data, or stop bits. The IrDA engine in the ’754C evaluate only single bits and only follow the 115.2 kbps protocol. The 115.2 kbps rate is a maximum rate. When both ends of the transfer are set up to a lower but matching speed, the protocol still works. The clock used to code or sample the data is 16 times the baud rate, or 1.843 MHz maximum. To code a 1, no pulse is sent or received for 1-bit time period, or 16 clock cycles. To code a 0, one pulse is sent or received within a 1-bit time period, or 16 clock cycles. The pulse must be at least 1.6 µs wide and 3 clock cycles long at 1.843 MHz. At lower baud rates the pulse can be 1.6 µs wide or as long as 3 clock cycles. The transmitter output, Tx, is intended to drive a LED circuit to generate an infrared pulse. The LED circuits work on positive pulses. A terminal circuit is expected to create the receiver input, Rx. Most, but not all, PIN circuits have inversion and generate negative pulses from the detected infrared light. Their output is normally high. The '754C can decode either negative or positive pulses on Rx.

IrDA Encoder Function

Serial data from a UART is encoded to transmit data to the optoelectronics. While the serial data input to this block (Int_Tx) is high, the output (Tx) is always low, and the counter used to form a pulse on Tx is continuously cleared. After Int_Tx resets to 0, Tx rises on the falling edge of the seventh 16XCLK. On the falling edge of the tenth 16XCLK pulse, Tx falls, creating a 3-clock-wide pulse. While Int_Tx stays low, a pulse is transmitted during the seventh to tenth clocks of each 16-clock bit cycle.

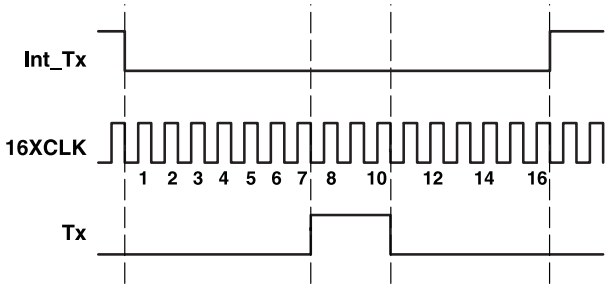


Figure 28. IrDA-SIR Encoding Scheme – Detailed Timing Diagram

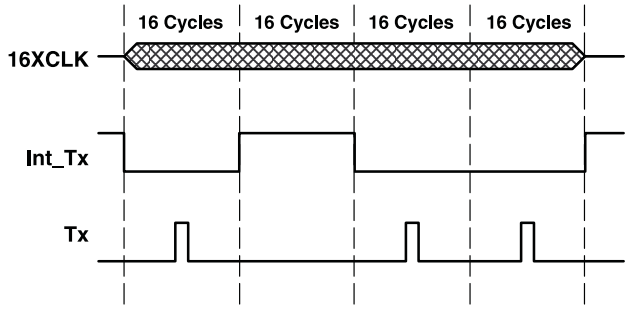


Figure 29. Encoding Scheme – Macro View

After reset, Int_Rx is high and the 4-bit counter is cleared. When a falling edge is detected on Rx, Int_Rx falls on the next rising edge of 16XCLK with sufficient setup time. Int_Rx stays low for 16 cycles (16XCLK) and then returns to high as required by the IrDA specification. As long as no pulses (falling edges) are detected on Rx, Int_Rx remains high.

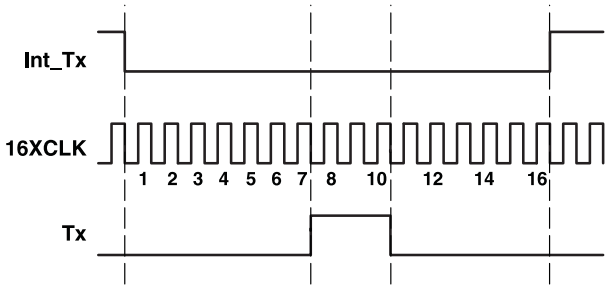


Figure 30. IrDA-SIR Decoding Scheme – Detailed Timing Diagram

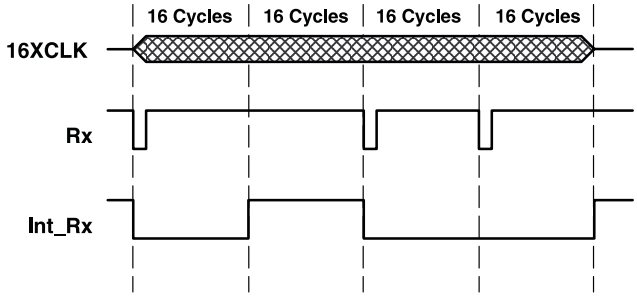


Figure 31. IrDA-SIR Decoding Scheme – Macro View

It is possible for jitter or slight frequency differences to cause the next falling edge on Rx to be missed for one 16XCLK cycle. In that case, a 1-clock-wide pulse appears on Int_Rx between consecutive zeroes. It is important for the UART to strobe Int_Rx in the middle of the bit time to avoid latching this 1-clock-wide pulse. The TL16C550C UART already strobes incoming serial data at the proper time. Otherwise, note that data is required to be framed by a leading zero and a trailing one. The falling edge of that first zero on Int_Rx synchronizes the read strobe. The strobe occurs on the eighth 16XCLK pulse after the Int_Rx falling edge and once every 16 cycles thereafter until the stop bit occurs.

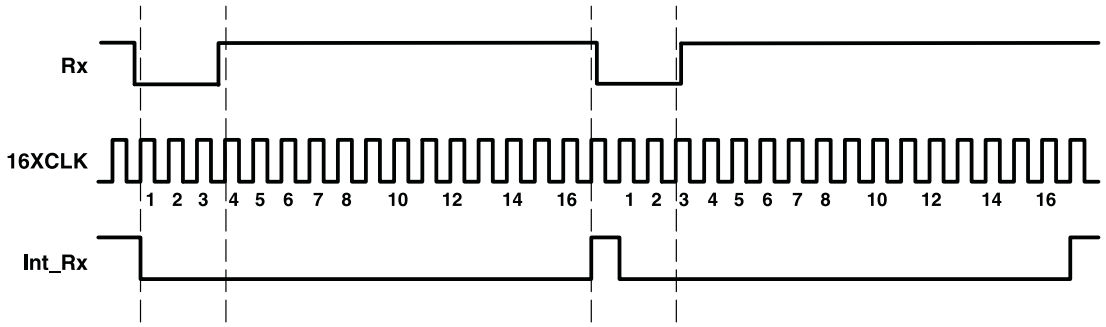


Figure 32. Timing Causing 1-Clock-Wide Pulse Between Consecutive Ones

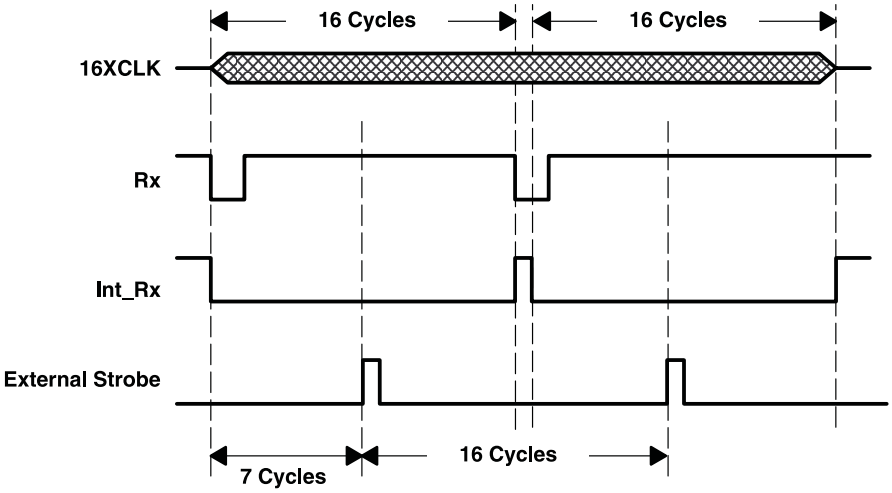


Figure 33. Recommended Strobing For Decoded Data

The '754C can decode positive pulses on Rx. The timing is different, but the variation is invisible to the UART. The decoder, which works from the falling edge, now recognizes a zero on the trailing edge of the pulse rather than on the leading edge. As long as the pulse width is fairly constant, as defined by the specification, the trailing edges should also be 16 clock cycles apart and data can readily be decoded. The zero appears on Int_Rx after the pulse rather than at the start of it.

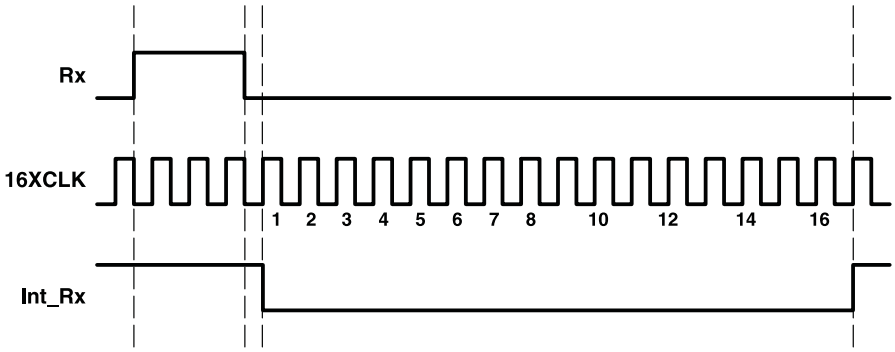


Figure 34. Positive Rx Pulse Decode – Detailed View

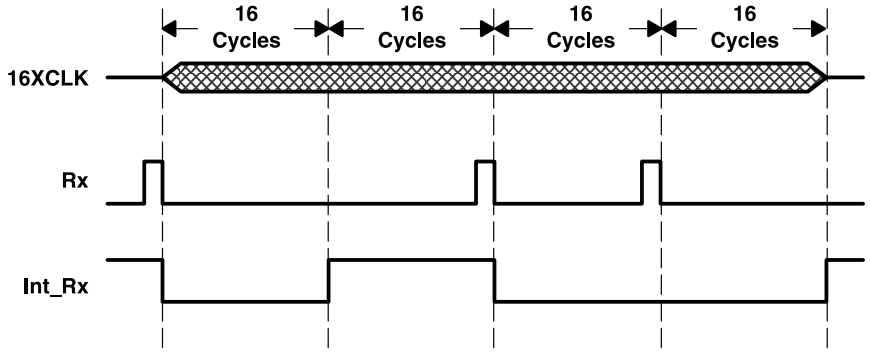


Figure 35. Positive Rx Pulse Decode – Macro View

TL16CP754C/TL16CM754C/TL16C754C Programmer's Guide

The base set of registers that are used during high speed data transfer have a straightforward access method. The extended function registers require special access bits to be decoded along with the address lines. The following guide will help with programming these registers. Note that the descriptions below are for individual register access. Some streamlining through interleaving can be obtained when programming all the registers.

Set baud rate to VALUE1,VALUE2	Read LCR (03), save in temp Set LCR (03) to 80 Set DLL (00) to VALUE1 Set DLM (01) to VALUE2 Set LCR (03) to temp
Set Xoff1,Xon1 to VALUE1,VALUE2	Read LCR (03), save in temp Set LCR (03) to BF Set Xoff1 (06) to VALUE1 Set Xon1 (04) to VALUE2 Set LCR (03) to temp
Set Xoff2,Xon2 to VALUE1,VALUE2	Read LCR (03), save in temp Set LCR (03) to BF Set Xoff2 (07) to VALUE1 Set Xon2 (05) to VALUE2 Set LCR (03) to temp
Set software flow control mode to VALUE	Read LCR (03), save in temp Set LCR (03) to BF Set EFR (02) to VALUE Set LCR (03) to temp
Set flow control threshold to VALUE	Read LCR (03), save in temp1 Set LCR (03) to BF Read EFR (02), save in temp2 Set EFR (02) to 10 + temp2 Set LCR (03) to 00 Read MCR (04), save in temp3 Set MCR (04) to 40 + temp3 Set TCR (06) to VALUE Set LCR (03) to BF Set EFR (02) to temp2 Set LCR (03) to temp1 Set MCR (04) to temp3
Set xmt and rcv FIFO thresholds to VALUE	Read LCR (03), save in temp1 Set LCR (03) to BF Read EFR (02), save in temp2 Set EFR (02) to 10 + temp2 Set LCR (03) to 00 Read MCR (04), save in temp3 Set MCR (04) to 40 + temp3 Set TLR (07) to VALUE Set LCR (03) to BF Set EFR (02) to temp2 Set LCR (03) to temp1 Set MCR (04) to temp3
Read FIFORdy register	Read MCR (04), save in temp1 Set temp2 = temp1 * EF Set MCR (04), save in temp2 Read FRR (07), save in temp2 Pass temp2 back to host Set MCR (04) to temp1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TL16CP754CIPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16CP754CIPMG4	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16CP754CIPMR	ACTIVE	LQFP	PM	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16CP754CIPMRG4	ACTIVE	LQFP	PM	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16CP754CPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16CP754CPMG4	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16CP754CPMR	ACTIVE	LQFP	PM	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16CP754CPMRG4	ACTIVE	LQFP	PM	64	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

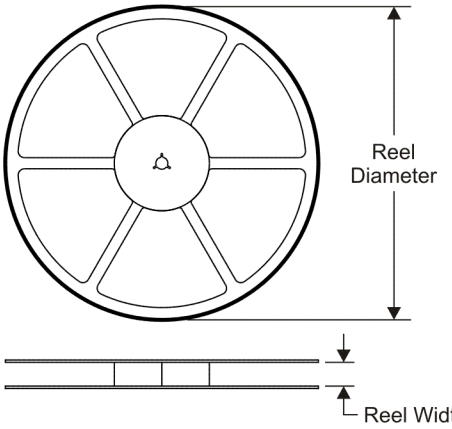
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

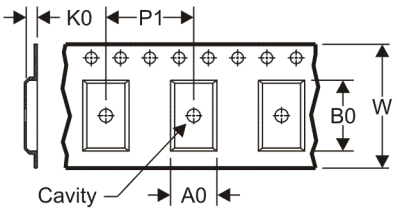
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

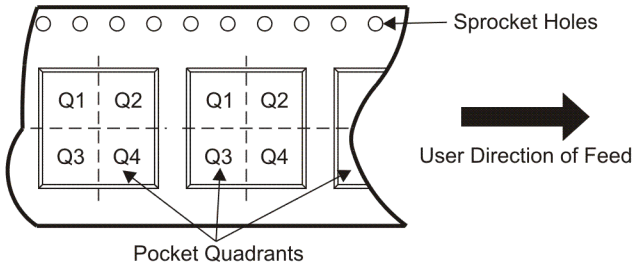


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

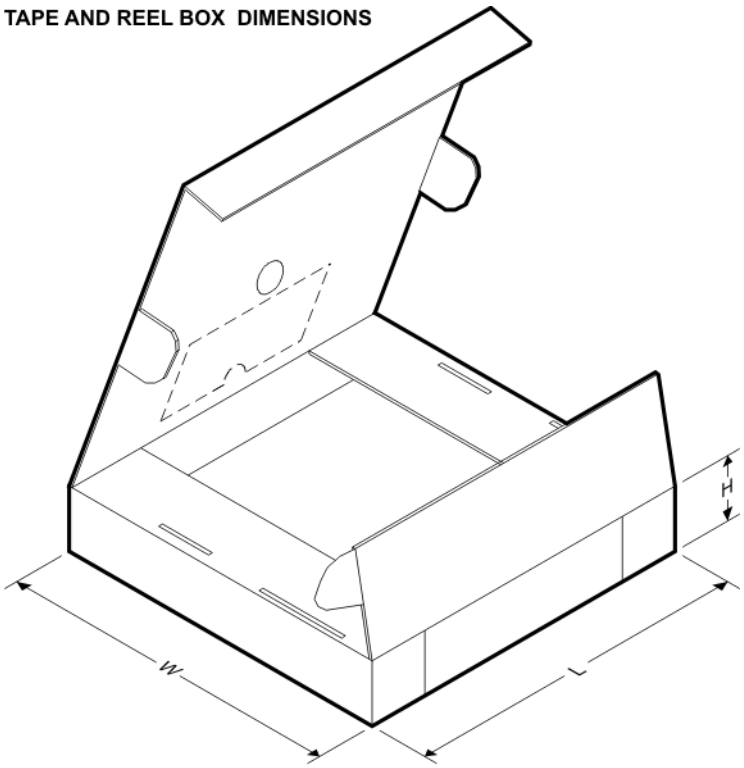
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL16CP754CPMR	LQFP	PM	64	2500	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2

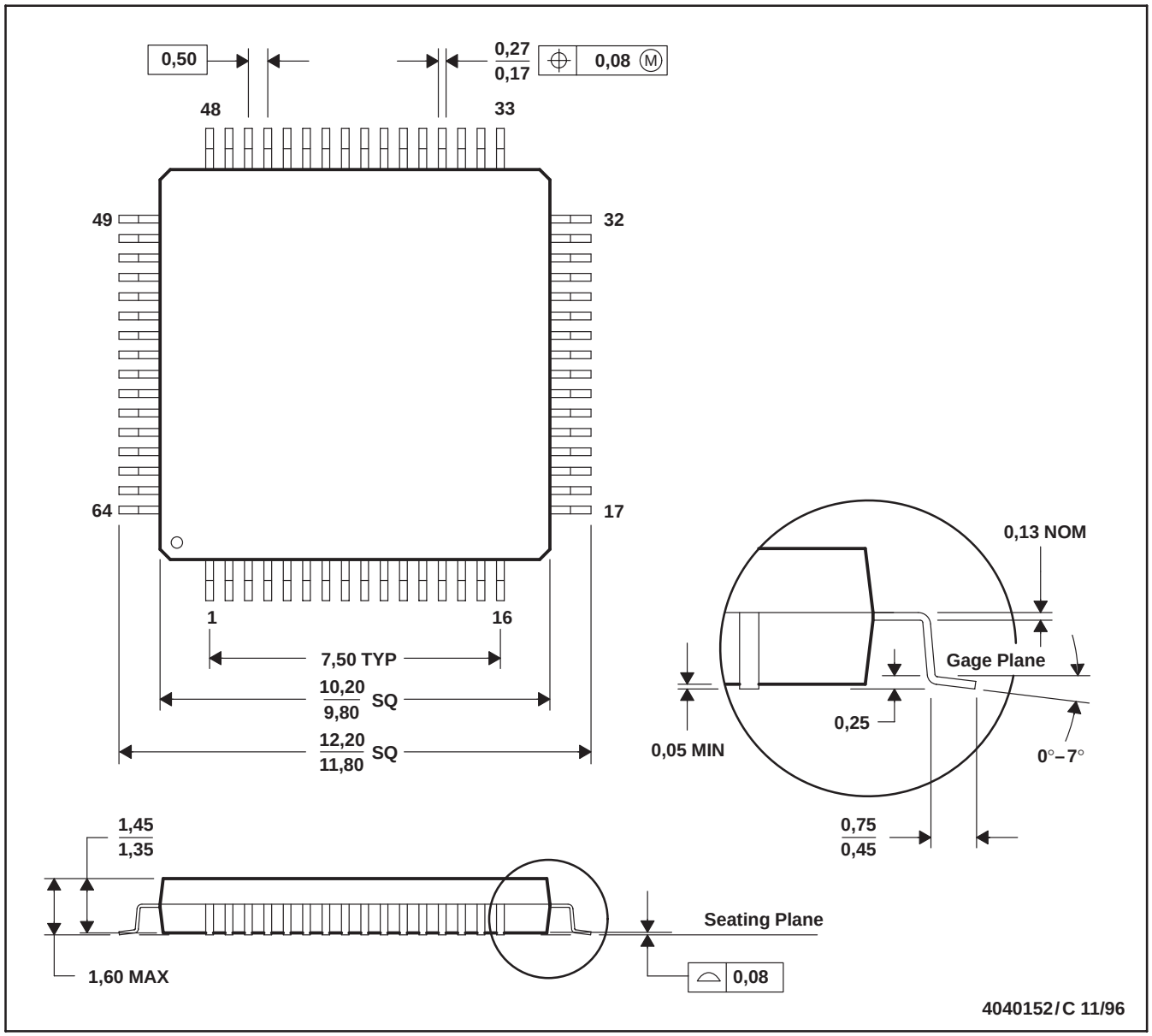
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL16CP754CPMR	LQFP	PM	64	2500	333.2	345.9	41.3

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265